

# Parametric study of optimum gate-resistance for performance and short-circuit robustness of novel half-bridge IGBT modules

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## Abstract

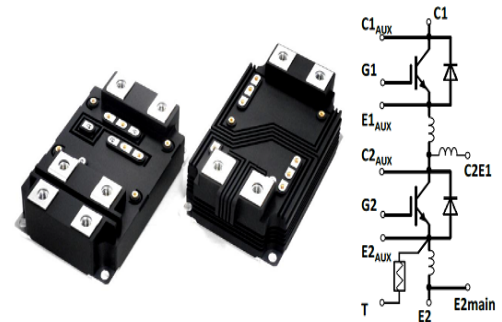
*This paper jointly investigates the switching performance and the short-circuit (S.C) turn off behavior of a novel half-bridge (2in1) IGBT power module concept with the low stray inductance ( $L\sigma$ ), which has been available in the market since 2015. Since this package was designed for improving the performance of Si-based switches and is a pioneering solution for designing WBG switches through reducing the  $L\sigma$  of the switch itself, investigations of S.C are an important task for both researchers and designers. The performance of a Half-bridge (2in1) Silicon N-channel IGBT has been examined with different temperatures, switching transients and testing under S.C conditions, where the extracted results offer a clear overview of S.C of Half-bridge (2in1) package and trade-offs between switch losses and short-circuit safe operating area (SCSOA), and finally prevention of false turn-on after short-circuiting due to  $L\sigma$ .*

**Keywords:** Half-bridge (2in1) module nHPD2, IGBT Robustness

## I. INTRODUCTION

In searching for low stray-inductance packages capable of utilizing semiconductors at the border of their limits whilst also commercializing wide-band-gap (WBG) semiconductors, manufacturers have been developing new open standard packages for Half-bridge (2-in-1) module platforms since 2016, modules are known commercially as nHPD<sup>2</sup>, XHP, LinPak and SemiTrans20. Designing half-bridge (2-in-1) package by semiconductor's manufacturers is a part of the optimization of circuit design solution in preventing large overshoot and ringing in WBG devices[13]. (2-in-1) half-bridge configurations have low inductance by narrowing the gap between p-n terminals gap, arranging terminals side by side [10]. and an <30nH stray inductance thanks to low stray inductance standard busbars for (2-in-1).

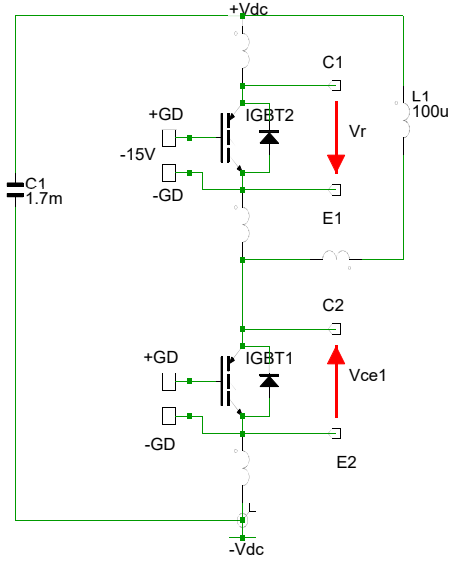
half-bridge, which make this package popular for high current and high voltage applications. The package appearance and an equivalent circuit are shown in Fig. 1.



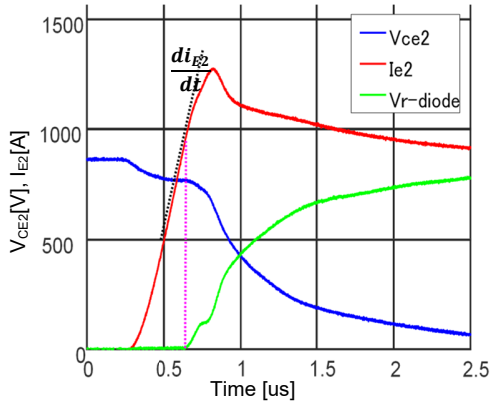
**Figure 1-Half bridge module package appearance and an equivalent circuit [4].**

Manufacturers claim that this new package provides around 30% higher power density and 75% less internal stray inductance when compared with conventional packages [1]. Experimentally, the maximum switch's loop stray inductance measured is 14.7nH shown in Fig. 3, which is slightly higher than what manufacturer claimed, the difference is probably because of different interconnects used for the measuring module's loop stray inductance. In this method the  $\frac{di_{E2}}{dt}$  was calculated when the high-side diode voltage been zero. At the same time  $V_{CE2}$  was measured, then  $L\sigma$  of module calculated through the expression demonstrated below Fig. 3.

the measuring method for calculating  $\frac{di_{E2}}{dt}$  and  $V_R$  shown Fig. 2.



**Figure 2. Measuring method for calculating  $\frac{di_{E2}}{dt}$  and  $V_R$  for calculating switch's stray Inductance( $L\sigma$ ) measurement method [9].**



$$l_{\sigma} = \frac{v_{CC} - v_R - v_{CE}}{\frac{di_{E2}}{dt}} = \frac{866.6 - 0 - 767.65}{6.7155e^9} = 14.735e^{-9}H \quad (1)$$

**Figure 3. Turn on wave form during Switch's  $L\sigma$  measurement,  $R_{G(on/off)} = 6.8\Omega/20\Omega$ , Room temperature**

Main target applications for Half-bridge (2-in-1) module are:

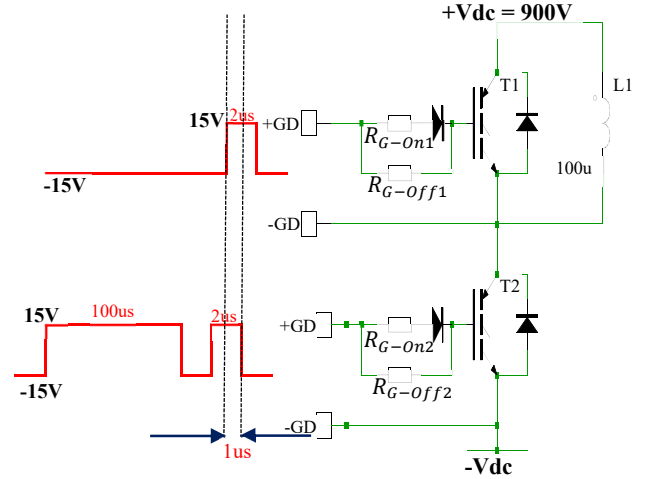
- Rail traction converters
- Aerospace converters
- Marine and offshore applications
- Automotive
- Solar converters and wind turbine converters

As reliability and fail-safe operation are highly recommended for these applications, the aim of the research

project is to examine mainly robustness performance of this new technology since this technology is nascent. In the late chapters we will discuss about S.C behavior of the mentioned module, then we will investigate the source for S.C oscillation and things to do to prevent turn off oscillation during S.C.

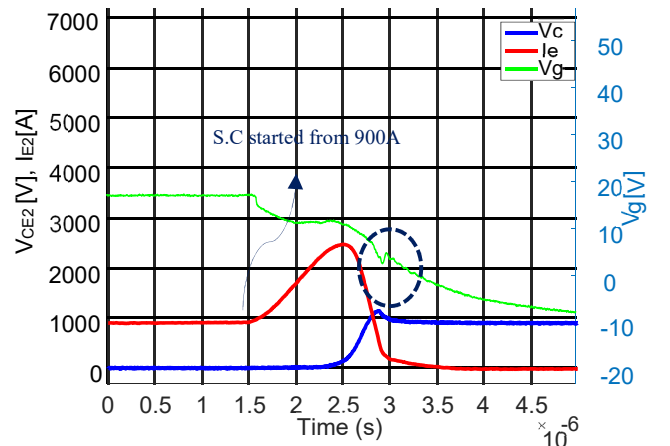
## II. SHORT-CIRCUIT TURN-OFF

Samples were examined with S.C type II (The configuration has been setup for a S.C test presented in Fig.4. The pulse of high-side and low-side overlapped within 1.5us) where the S.C started from 900A.



**Figure 3. Schematic illustration of test conditions for S.C type II (1us overlapping)**

The extracted waveforms have been reported in Fig. 4. 5. 6. 7. The amount of current passing through S.C module is inversely proportional to  $R_{G-off}$ , as  $R_{G-off}$  decreases the current the current rises steeply and in result during turn-off, large  $\frac{di}{dt}$  affects  $V_G$ . this fact shown in Fig. 5. 6. 7.



**Figure 4. S.C type II in case of  $R_{G-off}=15\Omega$ , Room temperature**

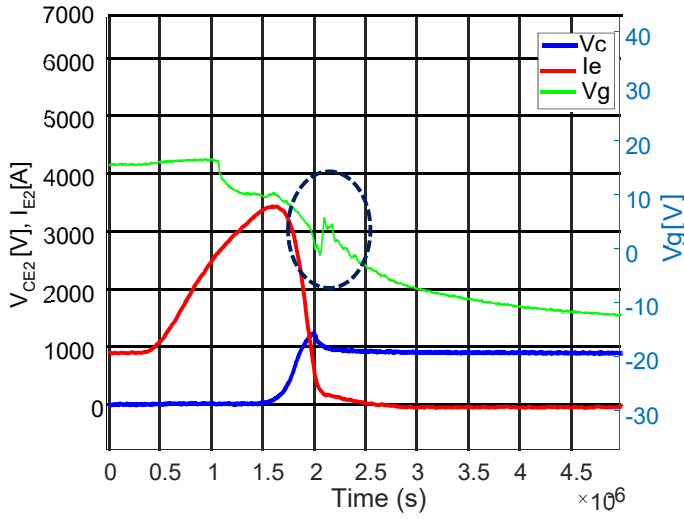


Figure 5. S.C type II in case of  $R_{G-off} = 10 \Omega$ , Room temperature

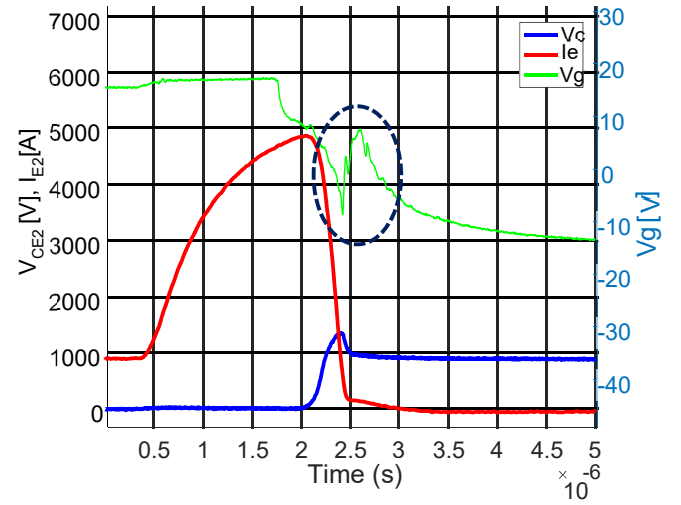


Figure 6. S.C type II in case of  $R_{G-off} = 4.9 \Omega$ , Room temperature

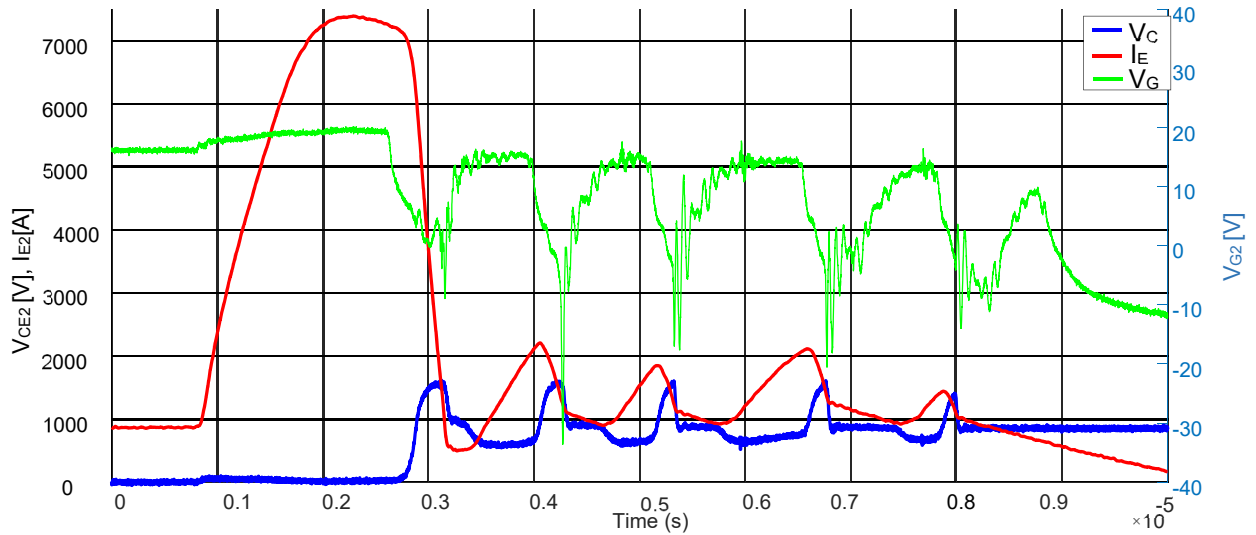


Figure 7. S.C type II in case of  $R_{G-off} = 2.7 \Omega$ , Room temperature

In the case of  $R_{G-off} = 2.7 \Omega$ ,  $V_{GE-LowSide}$  increases, until reaches threshold  $V_{GE-TH}$ , then switch involved a chain of parasitic oscillation shown Fig. 8.

### III. PARAMETRIC ANALYSIS OF OSCILLATORY BEHAVIOUR

Lower gate currents and/or higher gate resistances result in a slower voltage slope at turn-off. Thereby, the stored charge in the drift region of the IGBT is partly extracted and, thus,

the  $\frac{di_c}{dt}$  is increased. [6]. Switch-off transients for our DUT with different  $R_{G-off}$  shown Fig. 9.

Four types of failures in IGBT may occur during a S.C[12].

- 1- Electrical failure mode
- 2- Thermal failure mode
- 3- Turn-off failure mode
- 4- Leakage current induce failure mode.

Turn-off failure can be related to an excessive power surge involved in a voltage overshoot at the device turn-off. This

failure mode strongly depends on the  $R_G$  value and the collector stray inductance that governs the  $\frac{di}{dt}$  [12].

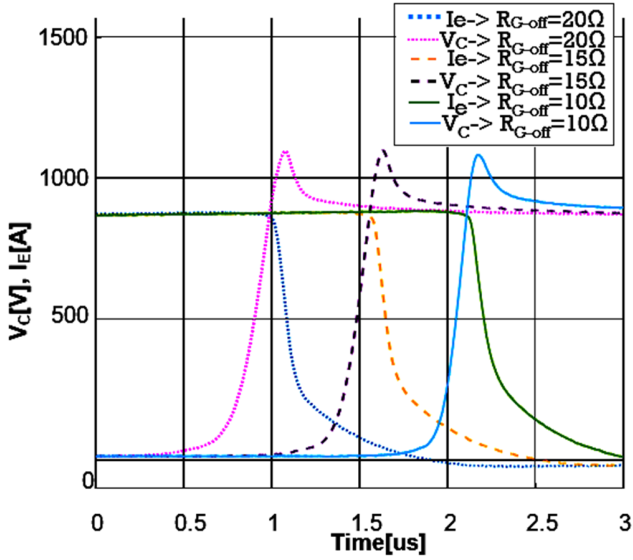


Figure 8. Switch off transients at different  $R_{G-off}$ , Room temperature

Also,  $E_{off}$  increases with increasing  $R_{G-off}$ , shown in Fig. 10. (Note that  $E_{off}$  been measured according to: “IEC60747–9 (2007) [3].

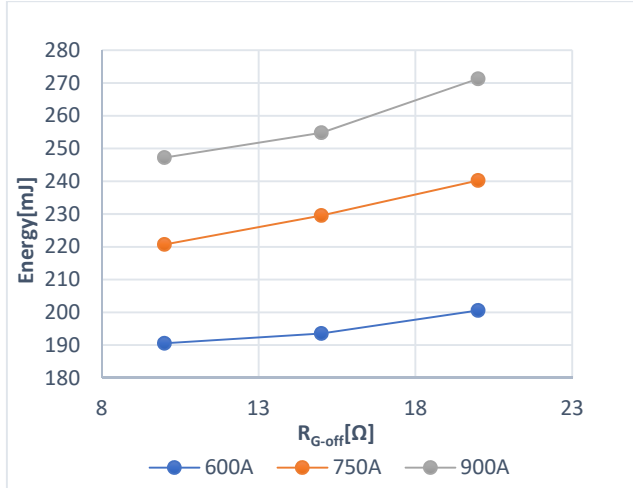


Figure 9.  $E_{off}$  vs  $R_{G-off}$  at different currents, Voltage = 900V, Room temperature

An IGBT may survive long S.C times but fail when turned off. Thus, an IGBT rated for long S.C time may fail at the turn-off simply due to the “dynamic latching.”, since the turn-off speed is to some degree dependent on the turn-off gate resistors [2].

There are two possible fast turn-on oscillations during S.C:

- False turn – on via the Miller capacitance
- False turn – on via stray inductances

In both the cases that are somehow related to the input capacitance  $C_{ies}$ , the  $C_{ies}$  must be charged to the threshold voltage, after which the device begins to turn on, and if discharged to the plateau voltage the device begins to turn off.

### III-I FALSE TURN-ON VIA THE MILLER CAPACITANCE

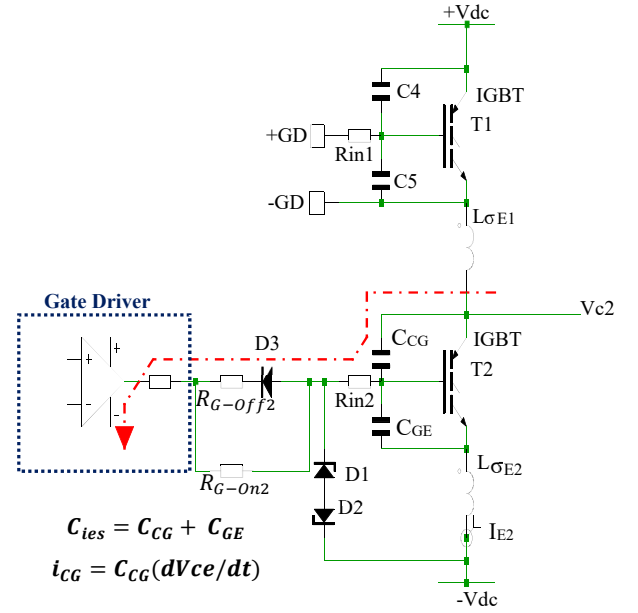


Figure 10. The parasitic capacitance current path low-side IGBT during parasitic Miller capacitance switching

A large voltage overshoot on  $V_{CE}$  induces a current into the Miller capacitance and raises the voltage of  $V_{GE}$ . The parasitic capacitance current path low-side IGBT during parasitic Miller capacitance switching Shown Fig. 10. Also, when turning off the lower IGBT in a half-bridge during S.C  $\frac{dv_{CE}}{dt}$  occurs across the upper IGBT diode. This current will pass through the Miller capacitance and then passes through  $R_G$ . If the voltage drop reaches the threshold voltage, a false turn-on will occur.

Neglecting the influence of the gate driving circuit, the gate-emitter voltage can be calculated by [8].

$$V_G = \frac{C_{GC}}{C_{GC} + C_{GE}} \cdot \Delta V_{CE} = \frac{C_{res}}{C_{ies}} \cdot \Delta V_{CE} \quad (2)$$

Where:

$C_{res}$ : reverse transfer capacitance

$C_{ies}$ : input capacitance

$\Delta V_{CE}$ : collector – emitter voltage

### III-II FALSE TURN-ON VIA STRAY INDUCTANCES

The effect of the Emitter inductance leads to an overshoot on the Collector current  $I_C$  coinciding at the same time with the highest voltage drop at the Collector-Emitter voltage  $V_{CE}$ . The combination of high Collector current and low Collector-Emitter voltage seems to be correlated with the occurrence of Gate-voltage oscillations under the short-circuit event [11].

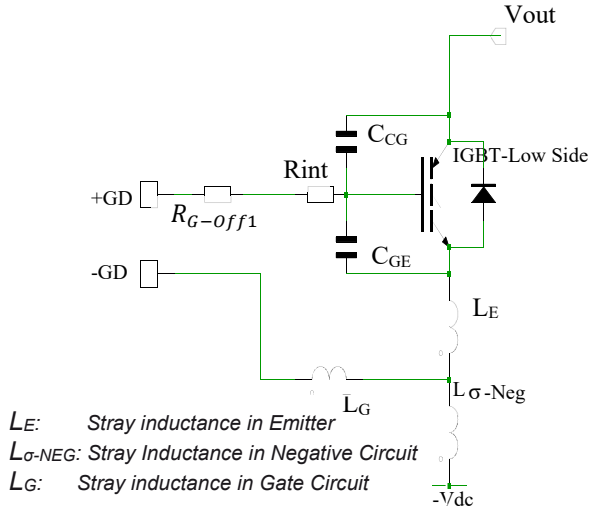


Figure 11. The equivalent circuit of Gate Drive Loop inductance of low-side IGBT [5].

The equivalent circuit of Gate Drive Loop inductance of low-side IGBT shown Fig. 12. When a large current is created by short-circuiting, turn-off will occur with large  $\frac{di}{dt}$ . This induces a voltage equal to  $L_{\sigma} \frac{di}{dt}$  in the circuit stray inductances. This voltage overshoot, if too large, would cause a chain of false switching, resulting in failure due to an excessive power surge or latching.

This mode of failure could be avoided by minimizing the circuit stray inductances on the DC side of the switching device, also called “DC loop” inductance. The objective could also be achieved by slowing the rate of fall of fault current, which again some degree is dependent on the turn-off series Gate resistor,  $R_{G-off}$  [2].

If consider  $C_{GE}$  is fixed:

$$V_{GD}^+ = (R_{off} + R_{int}) \cdot C_{GE} \cdot \frac{dV_{C_{GE}}}{dt} + \frac{Q_{GE}}{C_{GE}} + L_E \cdot \frac{d^2 V_{C_{GE}}}{dt^2} + L_{\sigma-NEG} \cdot \frac{di_{L_{\sigma-NEG}}}{dt} \quad (3)$$

$$V_{GD}^- = L_G \cdot \frac{di_{L_G}}{dt} + L_{\sigma-NEG} \cdot \frac{di_{L_{\sigma-NEG}}}{dt} \quad (4)$$

$$\text{Now: } V_{GD} = V_{GD}^+ - V_{GD}^- \quad (5)$$

$$V_{GD} = (R_{off} + R_{int}) \cdot C_{GE} \cdot \frac{dV_{C_{GE}}}{dt} + \frac{Q_{GE}}{C_{GE}} + L_E \cdot \frac{d^2 V_{C_{GE}}}{dt^2} - L_G \cdot \frac{di_{L_G}}{dt} \quad (6)$$

Since -16 V is applied to  $V_{GD}$  during turn-off:

$$-16V = (R_{off} + R_{int}) \cdot C_{GE} \cdot \frac{dV_{C_{GE}}}{dt} + \frac{Q_{GE}}{C_{GE}} + L_E \cdot \frac{d^2 V_{C_{GE}}}{dt^2} - L_G \cdot \frac{di_{L_G}}{dt} \quad (7)$$

$$-16V - (R_{off} + R_{int}) \cdot C_{GE} \cdot \frac{dV_{C_{GE}}}{dt} = \frac{Q_{GE}}{C_{GE}} + L_E \cdot \frac{d^2 V_{C_{GE}}}{dt^2} - L_G \cdot \frac{di_{L_G}}{dt} \quad (8)$$

If we call the gate node on substrate  $V_{G-SUB}$ :

$$V_{G-SUB} = \frac{Q_{GE}}{C_{GE}} + L_E \cdot \frac{d^2 V_{C_{GE}}}{dt^2} - L_G \cdot \frac{di_{L_G}}{dt} \quad (9)$$

$$V_{G-SUB} = -16V - (R_{off} + R_{int}) \cdot C_{GE} \cdot \frac{dV_{C_{GE}}}{dt} \quad (10)$$

Where:

$C_{GE}$ : Gate – Emitter capacitance

$Q_{GE}$ : charge stored on Gate – Emitter

$R_{int}$ : internal resistance of the Gate circuit

$R_{off}$ : ext turn – off resistance of the Gate driver

$V_{GD}^+$ : Gate driver positive voltage

$V_{GD}^-$ : Gate driver reference voltage

$V_{GD}$ : Gate driver overall voltage

$V_{G-SUB}$ : Gate substrate node voltage

$L_E$ : Stray inductance in Emitter

$L_{\sigma-NEG}$ : Stray Inductance in Negative Circuit

$L_G$ : Stray inductance in Gate Circuit

### IV. DEALING WITH TURN-OFF OSCILLATION

From (2) we understood that to prevent parasitic Miller capacitance switching, the quotient  $\frac{C_{res}}{C_{ies}}$  should be as low as possible it could be achieved simply by adding an external  $C_{GE}$  to low-side IGBT.

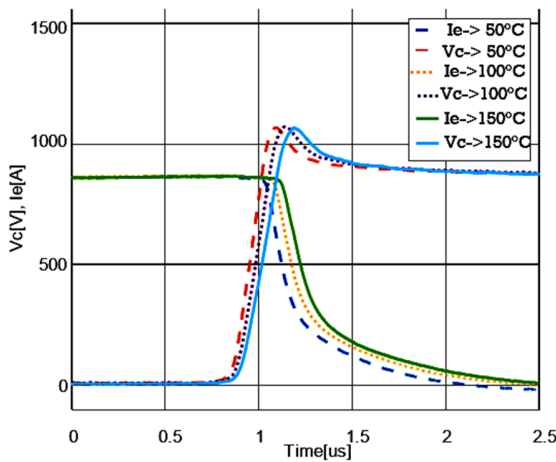
From (6) it is understood that  $V_{GD}$  does not depend to  $L_{\sigma-NEG}$  (Stray Inductance in Negative Circuit) during false turn-on via stray inductance after S.C, but it depends on Gate loop module's Internal Stray Inductance  $L_G$ , including Emitter stray inductance  $L_E$  and Gate Emitter capacitance  $C_{GE}$ .

From (10) we can conclude that by increasing  $R_{G-off}$  we are increasing the negative voltage applied to  $V_G$  substrate. Hence, to prevent parasitic turn-on due to  $L\sigma$  after S.C we must choose a value bigger than  $2.7\Omega$ .

From (2) and (10) by adding an external  $C_{GE}$  we can prevent parasitic turn-on after S.C due to stray inductance and Miller capacitance same time.

Although half-bridge IGBT modules manufacturers recommended  $100\Omega$  for  $R_{G-off}$ , but in searching an optimized value and the minimum value, the values for  $R_{G-off}$  during our tests have been chosen much less than this value (from  $15\Omega$  to  $2.7\Omega$ ) to examine the limits of  $R_{G-off}$ .

Since the  $E_{off}$  unaffected by the temperature during our experiments, this means that turn-off oscillations happened independently of module's temperature. Turn-off transients for different temperatures are shown in Fig. 12.



**Figure 12. Switch off transients at different temperature,  $R_{G(on-off)}=2.7\Omega/10\Omega$**

Note that in our samples even though the device started parasitic switching during S.C, but never involved dynamic latched up since upper thyristor never activated during the short circuit. It proves our samples were well designed in the Physical stage [7].

## CONCLUSION

In this paper, half-bridge (2-in-1) IGBT modules switching performance and robustness were examined using

a realistic scenario (S.C type II). The effect of  $R_{G-off}$  on short-circuit illustrated.  $V_{GD}$  relations during false turn-on via stray inductance has been extracted and shown that it does not depend on  $L_{\sigma-NEG}$ . Also, it was demonstrated why with increasing the  $R_{G-off}$  the chance of involving parasitic oscillation decreases, it was concluded it is sufficient to select  $R_{G-off}$  higher than  $2.7\Omega$  to prevent turn-off oscillation due to stray inductance after S.C; the value is fully compatible with optimum switching performance for half-bridge IGBT module and it doesn't need an ulterior consideration. Future work could be directed at investigating the dependency of switching frequency and S:C oscillation. Also, proposed to investigate an optimum external  $C_{GE}$  to prevent parasitic turn-on after S.C as one solution for both of stray inductance and Miller capacitance.

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