Thermal Analysis of High Power High Voltage DC Solid State Power Controller (SSPC) for Next Generation Civil Tilt Rotor-craft

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Abstract—**This paper explores different possible topologies of a high-power high-voltage bidirectional DC solid state power controller (SSPC) for aerospace applications. The most suitable topology is then selected for design and implementation of the SSPC. A detailed analytical thermal model of the most preferred SSPC is presented in this paper. Using the thermal model, the junction temperatures of the potential IGBT and MOSFET modules selected for the SSPC design are estimated during nominal and over-current situations. The prediction of the semiconductor device's junction temperature is of major significance during the design process of the SSPCs to ensure thermal stability during over-current situations. Later, a thermal model of the SSPC is built in a computer simulation software named PLECS and the junction temperature of the devices are evaluated for nominal and all over-loading conditions. In addition, the overall efficiency, weight, and power density of the SSPCs with respect to the selected devices are approximated. The device that exhibits better thermal resilience and good power density is selected for the future development of the DC SSPC for more electric aircraft.**

Index Terms—**Solid state power controller (SSPC), Conduction loss, Thermal stability, Junction temperature**

I. INTRODUCTION

The main concept behind more electric aircraft (MEA)/all-electric aircraft (AEA) is to replace non-electrical sources, transmission, and loads with the electrical ones. The new electrical architectures for MEA exhibit better efficiency, minimal weight, flexible load location, reduced volume, decreased noise/vibration, and increased reliability than that of the existing conventional architecture [1]–[4]. However, many advancements on MEA architectures are still in research and development phase.

The project INSTEP delivers a new electrical power system (EPS) for next-generation civil tilt rotorcraft (NextGen CTR). The EPS for CTR is based on new $\pm$ 270 V DC distribution system. The proposed architecture consists of three 90 kW generators and two 50 kW generators (with rectifiers) connected to $\pm$ 270 V DC bus. The DC bus acts as the main transmission system within the rotor-craft. Additional power electronic converters (PECs) along with circuit breakers are employed for interfacing different AC/DC loads and batteries.

One of the major challenges for the development of EPS is the design of suitable circuit breakers for high current and high voltage DC system. Traditional electromechanical circuit breakers (ECB) used in AC based systems offers low on-state resistance with galvanic isolation. However, these ECBs are not suitable for DC application due to its inherent arching problem and limited life. In addition, ECB is bulky and

has a slower response time as compared to semiconductor-based solid-state power controllers (SSPC). The hybrid circuit breakers (HCB) makes use of both copper contact and semiconductor devices but poses design complexity [3], [5], [6]. The schematics of three different types of CBs are shown in Fig. 1.
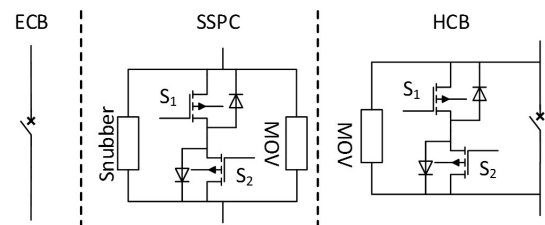

Fig. 1: Different types of circuit breakers used in electrical systems

Various types of solid state based circuit breakers and recent technological advancements in this field are over-viewed in [5]–[10]. In [5], the different types of semiconductor topologies for the SSPC along with design challenges are presented. The SSPC based on SiC devices for low current applications are experimentally verified in [7]. Solid-state based circuit breakers for microgrid applications are described in [6], [8]. High-voltage and high-power based SSPC on static induction transistor (SIT) devices are demonstrated in [10].

The SSPC is a 'normal on' switch carrying current throughout its life. In addition, the breaking current of the SSPC is 8-10 times higher than the nominal current [5]. Therefore, detailed thermal analysis of the SSPC during nominal and over-current situations needs to be explored. In this paper, various possible semiconductor topologies of the SSPCs are explained. Then, suitable semiconductor devices are selected for the most preferred topology and their thermal stability are analyzed. The estimation of device junction temperature is of great importance during the design process of the SSPC. The SSPC should ensure to flow nominal current for infinite time and over-currents for different time durations without thermally damaging its components. Section II outlines various types of SSPC topologies that can be used for bidirectional DC applications. The description of the studied SSPC is presented in Section III. Device selection and analytical thermal computations of the device's junction temperature are explained in Section IV. The validations of the analytical results with PLECS simulations are reported in Sections V.
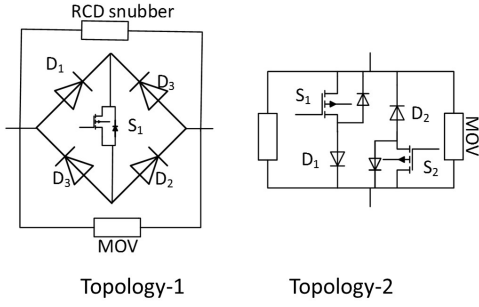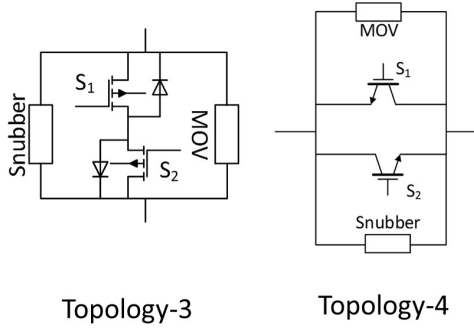
Fig. 2: Topology-1 and 2 of SSPC

Fig. 3: Topology-3 and 4 of SSPC

II. SEMICONDUCTOR TOPOLOGIES FOR BIDIRECTIONAL DC SSPCS

The SSPC can be realized with various topologies of the semiconductor devices. Some of the topologies considered in the literature are shown in Figs. 2 and 3. The comparison of these four topologies of the SSPCs is presented in Table I. Topology-3 is the most suitable topology for NextGen CTR EPDS since it allows the use of various semiconductor devices (MOSFET/IGBT/JFET) in either single or multiple channel configurations.

III. BIDIRECTIONAL DC SSPC FOR NEXTGEN CTR

The schematic circuit for the SSPC design for NextGen CTR shown in Fig. 4 consists of voltage source, transmission impedance, SSPC, and RC load. The design specifications of the DC SSPC are mentioned below:

- Nominal voltage rating: $\pm$ 270 V

TABLE I: Comparison of various types of SSPC topologies

	Topology-1	Topology-2	Topology-3	Topology-4
Device types	Diode +MOSFET	Diode +MOSFET/IGBT	MOSFET/IGBT	IGBT/ SiC BJT
Device count	5	4 (2)	2	2
Conduction loss	High	Moderate	Moderate	Low
Current Level	Low	Low	High	High
Channels	1	1	Single/Multiple	Single/Multiple
Driver Type	Voltage control	Voltage control	Voltage control	Voltage/Current Control

- Nominal Current rating: $\pm$ 170 A
- Pulse current rating: $\pm$ 170x9 A (1530 A for 3 ms), $\pm$ 170x5 A (850 A for 500 ms), $\pm$ 170x2 A (340 A for 2 sec)

From the design specification of the DC SSPC, the approximate I^2t tripping curve is generated and presented in Fig. 5. The pulse current requirement of this SSPC is higher than offered by commercially available SSPCs [5].
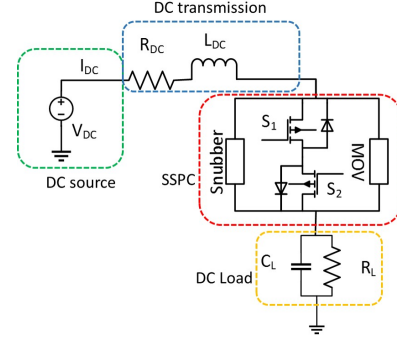

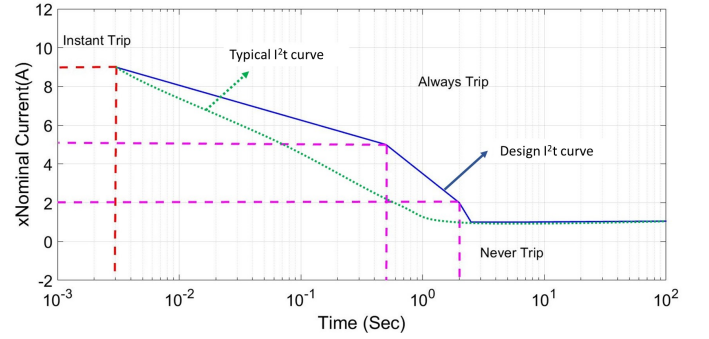**Fig. 4:** Schematic circuit with source, load, and the SSPC

Fig. 5: The derived I^2t curve for the proposed DC SSPC compared with typical I^2t curve of commercially available SSPC

For the transient and thermal simulation studies, assumed line and load impedances are mentioned below:

- DC transmission Line Impedance: R_{DC}= 0.1 $m\Omega$, L_{DC}=100 μH [11]
- Nominal Load: R_L=1.588 Ω $m\Omega$, C_L=100-1000 μF

IV. THERMAL ANALYSIS OF THE SSPC

A. Semiconductor Devices for the SSPC

The design criteria for DC SSPCs are:

- Being able to handle the nominal current and specified over-load currents without exceeding maximum junction temperature (T_{jmax})
- Min voltage stress (540 V)
- Operating ambient temperature is considered to be 85 $^\circ C$

For this application, high current MOSFETs/IGBTs are selected with voltage rating more than 1200 V. The basic device selection criteria are mentioned below:

- Minimum switch voltage (2x540 V)
- Minimum on-state resistance

MOSFET/JFETs are very useful for low current SSPCs and these semiconductor devices can be paralleled for achieving higher current rating. The paralleling operation eventually

reduces the conduction loss and each parallel channel can be used for different loads. However, additional parallel devices ask for additional drivers and heat sinks which impact the power density of the SSPC. On the other hand, IGBTs are effective for single channel SSPC with slower response. In addition, low cost, mature technology, high voltage and current ratings with good thermal characteristics make IGBT a good choice for high power SSPC. A comprehensive comparison study of MOSFET-based SSPC and IGBT- based SSPC with topology-3 is introduced in the following section.

Three MOSFETs currently available on the market (APT100MC120JCU2-ND-Microsemi, CAS325M12HM2-CREE, and CAS300M12BM2-CREE) with low on-state resistance are selected for the design of the DC SSPC in this project. The various ratings and details of the selected devices can be found onCREE and Microsemi official websites [12]–[14]. For applications where the voltage requirement is over 600V, no silicon MOSFET/JFET are available for higher current rating. Therefore, all selected MOSFETs are silicon carbide (SiC) MOSFETs which are several times expensive than ordinary MOSFETs.

While paralleling the IGBTs, one of the parallel loop may get overheated due to improper heat dissipation. The on-state resistance of the overheated IGBT decreases which will increase the magnitude of current flowing through it. This phenomenon continues till the junction temperature of the overheated IGBT reaches its limit. Therefore, the paralleling of the IGBTs is not preferred. So, IGBTs with high current ratings are chosen for this application. Three IGBTs (CM1400HA-24-Mitsubishi, FZ900R12KP4-Infenion, and FZ1600R17HP4_B2-Infenion) are selected for this application. The specification of these three IGBTs can be found in [15]–[17].

B. Thermal analysis of semiconductor devices during steady state

A simplified thermal circuit of the semiconductor device is illustrated in Fig. 6 [18]. The junction to case thermal impedance (R_{thjc}) is the intrinsic parameter of the device which can not be changed with external circuit design and heat sink. However, the case to the ambient thermal impedance (R_{thca}) depends on the size of heat-sink and grease/paste used between the heat-sink and the case.
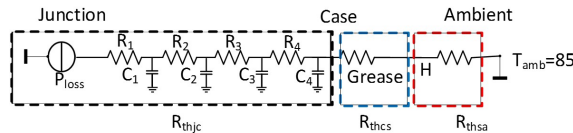

Fig. 6: Thermal circuit of semiconductor device

The size/shape/material of the sink determines the physical current limit of the semiconductor device. The maximum heat loss (P_{max}), steady state drain current for MOSFET ($I_{d(mos)}$) and IGBT ($I_{d(igbt)}$) as the function of thermal resistance of the heat-sink are given by eqns. (1), (2), and (3) [5], [19], [20]:

$$P_{max} = \frac{T_j - T_a}{R_{thja}} \tag{1}$$

$$I_{d(mos)} = \sqrt{\frac{T_j - T_a}{R_{thja} R_{dson(max)}}} \tag{2}$$

$$I_{d(igbt)} = \sqrt{\frac{T_j - T_a}{R_{thja} \frac{\Delta V_{ce(sat)}}{\Delta I_d}}} \tag{3}$$

where T_j and T_a are operating junction temperatures and ambient temperature in $^\circ C$, respectively. The parameters, $R_{dson(max)}$ and R_{thja} is the maximum on-state resistance of the device and thermal resistance from junction to ambient, respectively.

The main parameters that determine the physical current limit of the devices are the cumulative thermal resistance from device's junction to the ambient. The different heat sinks proposed for the calculation of theoretical current limit are listed in Table II.

TABLE II: Heat sink parameters for a theoretical physical current limit of the devices

S.No	Parameters	Microsen Device	Cree Devices	IGBTs
1	Sink Dimension (mmxmmxmm)	54x54x20	165x165x65	165x165x65
2	Sink material	Al	Al	Al
3	R_{thha} $^\circ C$/W at fan speed 0 m/s	6	0.57	0.57
4	R_{thha} $^\circ C$/W at fan speed 1 m/s	1.6	0.12	0.12
5	R_{thha} $^\circ C$/W at fan speed 2 m/s	0.9	0.085	0.085
6	Weight (gm)	30	808	808

Using the datasheets of the devices provided in previous tables and sink thermal resistance, the maximum power dissipation limit and physical drain current limit of the selected devices are calculated. The value of drain current in less than the specified maximum current limit in the datasheet. This is due to the high ambient temperature (85 $^\circ C$) around the device and finite heat sink to dissipate the loss-power.

Since, the steady state current of the SSPC is higher than that of physical current limit of the devices in case of MOSFETs. There, multiple channels of the MOSFETs need to be paralleled to match the current rating. The number of channel (n) required can be expressed as [5]:

$$n \cong \sqrt{\frac{I_{dc}^2 R_{dson(max)} R_{thja}}{T_j - T_a}} \tag{4}$$

After paralleling multiple MOSFET matrix, the junction temperature should not exceed the maximum junction temperature limit. The maximum junction temperature as a function of number of channels can be evaluated as [5]:

$$T_{j(act)} >= \frac{I_{dc}^2}{n^2} R_{dson(max)} R_{thja} + T_a < T_{j(max)} \tag{5}$$

For the IGBTs, the number of parallel loops can be approximated with the help of eqn. (6). However, the maximum number of channels necessary should be always less than one.

$$n \cong \frac{I_{dc}V_{cesat(max)}R_{thja}}{T_j - T_a} < 1 \qquad (6)$$

C. Thermal analysis of semiconductor devices during over-current situation

The rated breaking current of the SSPC is more than nine times the nominal current. Therefore, during tripping of the SSPC, the junction temperature may go beyond the maximum limit and eventually destroy the device. The transient thermal junction to case impedance of the device decides the transient increase in junction temperature during pulsating current.

TABLE III: Transient thermal impedance of devices

S.No	Parameters	APT100M C120JCU2-ND	CAS325 M12HM2	CAS300 0M12BM2
		MOSFETs		
1	R_{thjc} °C/W	0.7	0.127	0.076
2	Z_{thjc} °C/W for 3 ms	0.4	0.065	0.04
3	Z_{thjc} °C/W for 500 ms	0.7	0.127	0.076
4	Z_{thjc} °C/W for 2 s	0.7	0.127	0.076
		IGBTs		
		CM1400HA-24S	FZ900R12KP4	FZ1600 R17HP4_B2
1	R_{thjc} °C/W	0.05	0.078	0.0266
2	Z_{thjc} °C/W for 3 ms	0.0096	0.018	0.0045
3	Z_{thjc} °C/W for 500 ms	0.05	0.078	0.0266
4	Z_{thjc} °C/W for 2 s	0.05	0.078	0.0266

The minimum number of parallel channels required for the MOSFETs in order to withstand the transient current is expressed in eqn. (7). The maximum junction temperature during transient condition can be calculated using eqn. (8) [19], [20].

$$n \cong \sqrt{\frac{I_p^2 R_{dson(max)} Z_{thjc}}{T_j - T_c}} \qquad (7)$$

$$T_{j(act)} >= \frac{I_{dc}^2}{n^2} R_{dson(max)} Z_{thjc} + T_c < T_{j(max)} \qquad (8)$$

where Z_{thjc} and T_c are the transient thermal resistance and the case temperature of the devices.

The number of parallel loops required during and maximum junction temperature of the IGBTs during transient condition can be approximated as [19], [20]:

$$n \cong \frac{I_p V_{cesat(max)} Z_{thjc}}{T_j - T_c} < 1 \qquad (9)$$

$$T_{j(act)} >= I_p V_{cesat(max)} Z_{thjc} + T_c < T_{j(max)} \qquad (10)$$

where $V_{cesat(max)}$ is maximum on state voltage drop of the IGBT.

The number of MOSFET parallel loops are calculated for both steady-state and transient state. However, the higher 'n' (between steady-state and transient state) should be number of parallel loops for thermal stability. For Microsen MOSFET(APT100MC120JCU2-ND), the number of channels required to sustain very high peak current is more than 20 (as calculated using eqn. (7)) therefore, it would be very unreliable to develop SSPC with forty MOSFET devices. However, five channels are sufficient to build SSPC using high current CREE MOSFETs.

For any IGBT with a negative coefficient of resistance, the value of n should be always less than one and $T_{j(act)}$ should be always less than $T_{j(max)}$ of the device.

TABLE IV: Device count and junction temperature of the devices during different transient condition obtained analytically

S.No	Parameters	CAS300 M12BM2	CM1400 HA-24S	FZ900 R12KP4	FZ1600R1 7HP4_B2
1	Device counts (channel)	10 (5)	2 (1)	2 (1)	2 (1)
2	T_j with Nominal Current (°C)	125	120	120	115
3	T_j with 3 ms pulse (°C)	148	149	176	135
4	T_j with 500 ms pulse (°C)	131	171	201	148
5	T_j with sec pulse (°C)	122	145	159	134

The number of channels required and junction temperature (evaluated analytically) under various conditions for different semiconductor devices is listed in Table IV. High current CREE MOSFETs (CAS300M12BM2/CAS325M12HM2) are the most suitable for multichannel SSPC with the easier cooling mechanism. However, device counts are higher in order to meet the peak current rating of the SSPC.

Single channel SSPC can be designed using Mitsubishi IGBT (CM1400HA-24S), however, maximum junction temperature is just within the limit during the current spike. The Infineon IGBT (FZ1600R17HP4B2) exhibits better thermal stability than any other devices but is slightly bulkier and more expensive than other IGBTs of similar ratings. The other lighter and cheaper Infineon IGBT (FZ900R12KP4) cannot be used due to thermal instability during over-current operation and is not further included in the simulation.

V. THERMAL SIMULATION OF THE SSPCs

In order to validate the thermal stability of the SSPC, the thermal circuit of the SSPC is simulated using PLECS software. The device parameters and thermal data of the selected devices are embodied into the software. The over-current situation is created using programmable load. The ambient temperature of 85 °C is imposed on all semiconductor

devices and heat sinks. The PLECS simulation model of the SSPCs are then subjected to the all current/load situations as mentioned in Section II.

TABLE V: Junction temperature of devices during nominal and over-current situation obtained via PLECS modelling

S.No	Parameters	CAS300M12BM2 /CAS325M12HM2	CM1400 HA-24S	FZ1600 R17HP4_B2
1	R_{thca} in $^\circ C/W$	4	0.1	0.1
2	Maximum jun. tempr. 1 x nom. cur.	120	114	105
3	Maximum jun. tempr. 2 x nom. cur. (2 sec)	126	118	108
4	Maximum jun. tempr. 5 x nom. cur. (500 ms)	138	155	120
5	Maximum jun. tempr. 9 x nom. cur. (3 ms)	128	139	116
6	Maximum jun. tempr. staircase pulse	155	174	126

A single input/single output SSPC is designed with five internal channels using CREE MOSFETs. The conduction loss of the diode (second switch's antiparallel diode) is nil because the voltage drop across the diode is not sufficient to forward bias, and eventually no current flows through it. The maximum junction temperature during nominal condition reaches up to 120 $^\circ C$ with a heat sink (R_{thca}=4 $^\circ C$/W). Similarly, total loss per device is around 8.2 W. If two times of the nominal current flows through the SSPC, the junction temperature reaches up to 126 $^\circ C$.

Single channel IGBT based SSPCs are designed in PLECS using Mistubishi and Infineon devices for thermal analysis. The steady-state device junction temperatures for SSPCs notched up to 114 $^\circ C$ and 105 $^\circ C$, respectively for Mitsubishi and Infineon devices. The two-second over-current (two times of the nominal current) scenario is simulated with SSPCs based on the two different devices and the maximum junction temperature of the Mitsubishi device is 117 $^\circ C$ and Infineon device is 108 $^\circ C$ (with the heat sink, R_{thca}=0.1 $^\circ C$/W).

For 500 ms pulse, the magnitude of the over-current is five times of the nominal current, the junction temperatures surge high for devices with small case area. However, Infineon device provides the best thermal stability with a maximum junction temperature of 120 $^\circ C$.

The SSPC for this application is subjected to handle nine times of the nominal current for 3 ms. In addition, the worst case over-current scenario is created with all over-current staircase pulses (two consecutive staircase pulses (at 50 sec interval) of 2 times of the nominal current for 2 sec, 5 time of the nominal current for 500 ms, 9 times of the nominal current for 3 ms). The maximum junction temperatures obtained from simulation of the devices during all conditions are provided in Table V. The junction temperature of the devices obtained with simulation nearly matches the analytical results presented in the earlier section.

After two pulses of staircase over-current pulse, the max-

imum junction temperatures attained by the devices are 155 $^\circ C$, 174 $^\circ C$, and 126 $^\circ C$, respectively for CREE, Mitsubishi, and Infenion devices. Infenion device has more case area as compared with Mitsubishi/CREE's case area which allows Infenion device to easy heat dissipation during the transient condition. Moreover, it can withstand multiple over-current pulses than other devices without exceeding the junction temperature. A PLECs simulation result for CREE device is shown in Fig. 7, however other graphical results are omitted due to page constraints.
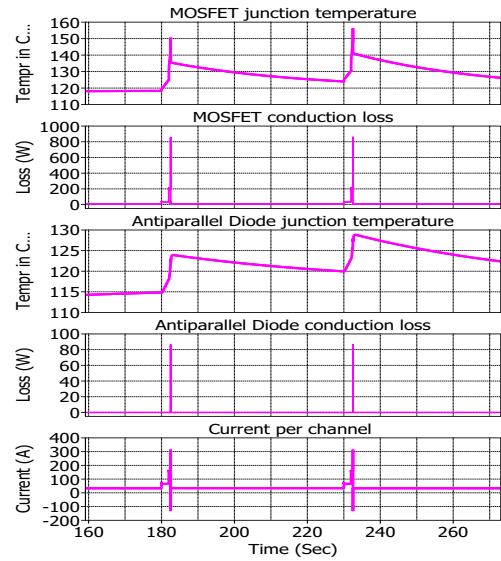
Fig. 7: Junction temperature and loss per device of CREE MOSFET used in SSPC design (staircase pulse)

VI. NOMINAL EFFICIENCY OF THE SSPC

The semiconductor devices of SSPCs are normally on throughout its life except breaking operations. Therefore, the major loss of the SSPC is the conduction losses. The switching loss of the device is ignored while evaluating the nominal efficiency of the SSPC during the design process.

The conduction loss of MOSFET based SSPC is the sum of conduction losses of two MOSFETs per channel. During a steady state of the CREE device, antiparallel diodes are never turned on due to the very low voltage drop across the MOSFET. So, conduction loss due to the antiparallel diode is omitted from the calculation. The conduction loss ($C_{l(mos(sspc))}$) and efficiency ($\eta_{mos(sspc)}$) of the MOSFETs based SSPC can be estimated as:

$$C_{l(mos(sspc))} = 2\frac{I_{DC}^2}{n}R_{dson(T_j(act))} \tag{11}$$

$$\eta_{mos(sspc)} = \left(1 - \frac{2I_{DC}}{nV_{DC}}R_{dson(T_j(act))}\right) \tag{12}$$

For IGBT based SSPC, the total loss is the summation of conduction loss of a IGBT and an antiparallel diode. The total conduction loss ($C_{l(igbt(sspc))}$) and efficiency ($\eta_{igbt(sspc)}$) of IGBT based SSPC can be approximated as:

$$C_{l(igbt(sspc))} = I_{DC}\{(V_{ce(sat-igbt)} + V_{ce(sat-diode)}\} \quad (13)$$

$$\eta_{igbt(sspc)} = \left(1 - \frac{I_{DC}\{(V_{ce(sat-igbt)} + V_{ce(sat-diode)}\}}{V_{DC}I_{DC}}\right) \quad (14)$$

The IGBT based SSPC consists of two IGBT modules and cooling fan based sinks. The weights of those sinks are approximately one kg per sink. However, SiC-MOSFET based SSPC module consists of ten modules with each sink weighing 300 gms. Therefore, the cumulative weight of semiconductors and their heat sinks in case of MOSFET based modules is higher than that of IGBT based modules. In addition, a large number of devices requires more drivers and other auxiliary powering circuits leading to more weight and cost of the overall system. However, the higher switching frequency of MOSFET allows faster tripping time than that of the IGBTs. The comparison of SSPCs based on semiconductor device used is presented in Table VI. Out of three main devices, Infineon IGBT, $FZ1600R17HP4\_B2$, would be a suitable selection for this application due to its reasonable good reliability, tripping time, cost, weight, and volume.

TABLE VI: Various parameters of SSPCs designed using different semiconductor devices

S.No	Parameters	CAS300M12BM2 /CAS325M12HM2	CM1400 HA-24S	FZ1600 R17HP4_B2
1	Min. Breaking time (us)	50	150	150
2	**Approx. weight (kg)**	**6 (4.5)**	**4**	**4.6**
3	Approx. power density (kW/kg)	15.2 (23.2)	23.5	20.4
4	Approx. volume (litre)	3.4 (3.1)	3.38	4.5
5	Approx. volume density (kW/litre)	26.25 (28.8)	26.4	19.84
6	Approx. cost (£)	4900 (10,000)	1200	2200
7	Approx. cost density (W/£)	18.3 (8.982)	74.4	40.5
8	**Efficiency in %**	**99.80 (99.82)**	**99.22**	**99.21**
9	Reliability	Low	Moderate	High

VII. CONCLUSION

Four different topologies of the SSPCs suitable for high power HVDC distribution in MEA are investigated. It is found that an SSPC designed with a matrix of semiconductor devices (two devices connected with a common collector) is flexible to use IGBT/MOSFET/JFET and can be used for various power range. Three MOSFETs and IGBTs are found suitable for the design and implementation of this high power SSPC. High current and high voltage CREE MOSFETs (CAS300M12BM2/CAS325M12HM2) needs five parallel channels to withstand transient current during turn-off. Two different IGBTs (CM1400HA-24S-Mitsubishi and FZ1600R17HP4_B2-Infineon) are suitable for single channel high power SSPC. It is found that five channel MOSFET based IGBT exhibits maximum efficiency, however, the power density of MOSFET based SSPC is lower than IGBT based SSPC. Out of these three devices, FZ1600R17HP4_B2 is found to be the most suitable due to high thermal stability, reasonably good efficiency, and better power density.

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