Unipolar Single Reference Multicarrier Sinusoidal Pulse Width Modulation Based 7-level Inverter with Reduced Number of Semiconductor Switches for Renewable Energy Applications

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***Abstract*—In the present scenario of increasing power demand and depletion of fossil fuel results in the research advancements in the field of renewable energy sources. Among various types of renewable energy sources, photovoltaic related applications are gaining importance. DC-AC converters play a very prominent role in photovoltaic system in efficient power delivering for various applications. This paper proposed a 7-level inverter with reduced number of switches for photovoltaic applications. Unipolar Single Reference Multicarrier Sinusoidal Pulse Width Modulation (U-SR-MC-SPWM) technique is used for the purpose of gate pulse generation for the proposed multilevel inverter. A comparative study of seven-level cascaded multilevel inverter and a proposed multilevel inverter is carried out. Simulation and power quality analyses of both multilevel inverters are performed in MATLAB/Simulink platform version 2016(a). It is noticed that the total harmonic distortion is slightly more of the proposed multilevel inverter when compared with cascaded h-bridge inverter. But, with the reduction in the number of power semiconductor switches in proposed multilevel inverter overall switching power losses, circuit complexity, gate driver requirements and cost of the system can be reduced. The simulation results always show a good agreement with the proposed approach.**

Keywords— Unipolar Single Reference Multicarrier SPWM, Cascaded Multilevel Inverter; Power Semiconductor devices, Renewable Energy, Total Harmonic Distortion (THD).

I. INTRODUCTION

Power generation using renewable energy sources is increasing in this present world due to the high demand of electrical power which plays a vital role in all the areas. Renewable energy-based power generation finds application in almost all sectors like industries, commercial areas, agricultural areas, etc. [1]-[2]. Due to the high rate of pollution and depletion threat on the fossil fuel, renewable energy sources are found as an alternative to the fossil fuels. All renewable energy sources are clean and sustainable energy sources. Solar photovoltaic, wind energy, biomass, ocean energy and geothermal are the important renewable energy sources. Among all the renewable energy sources the solar photovoltaic system [1]-[3] is having wide range of applications. Solar energy which is almost always available all time in a year can be effectively used for electrical power generation.

At present, various notable researches and developments are increasing in the field of solar photovoltaics [4]. Earlier days the high expense and low efficiency of photovoltaic systems made the public to stand away from this, but now due to excellent and fruitful researches in the area of material science have reduced the cost of solar modules and also improved the efficiency to a large extent. Power electronics are used anywhere where there is a need to process and conversion of electrical energy. Renewable power and power electronics are highly interlinked [1]-[4]. Power electronic interfaces are used in photovoltaic system for efficient power conversion processes. Various dc-dc and dc-ac power converters are basically used in photovoltaic systems [5]. As the photovoltaic systems are generating dc power, inverters are to be used for converting dc power to ac power. For single phase of grid photovoltaic application basically single phase full bridge inverters are being used. But for high power application multilevel multiphase inverters are preferred which is another recent trend in power electronics [6]-[10]. The output from full bridge inverters contain more harmonics are present.

The photovoltaic related applications are increasing at a fast rate in every sector where power demand is crucial [11]. Solar cells form the basic building element in all photovoltaic systems. Group of cells connected in series parallel combination results in the formation of solar modules and series parallel combination of modules has made solar panel. Solar photovoltaic systems are basically used in two ways as a standalone system and grid connected system [1]. It is well

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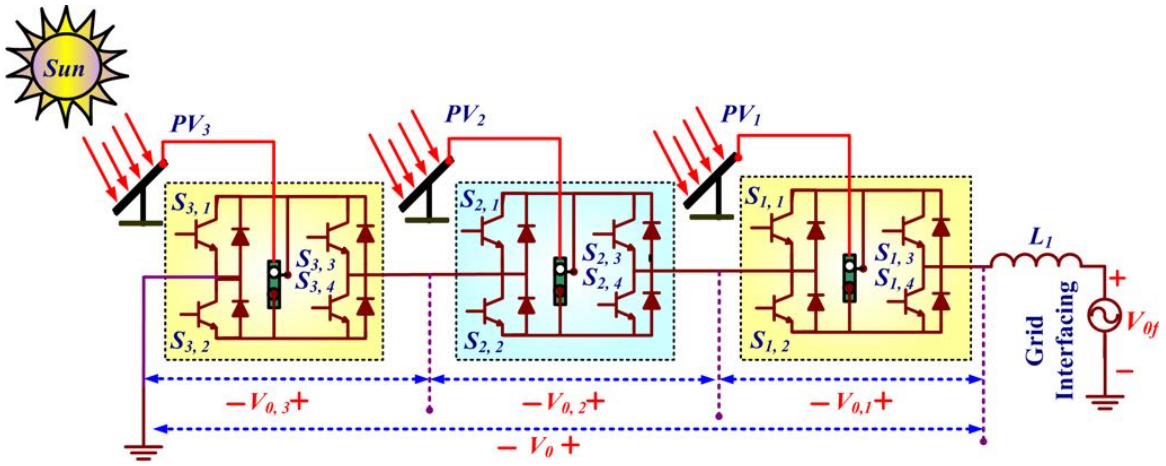


Fig. 1. Power Circuit of 7-Level Cascaded H-Bridge Converter.

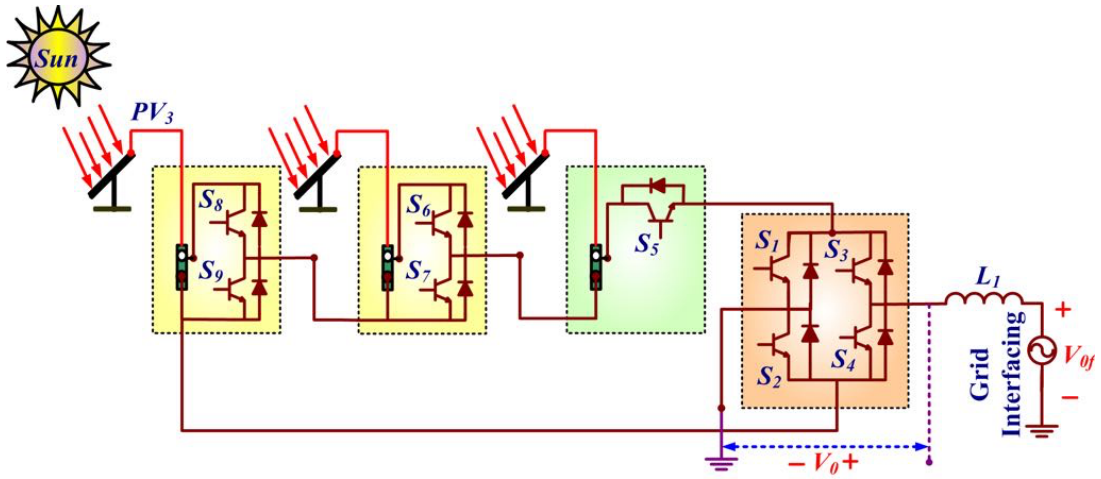


Fig. 2. Power Circuit of 7-Level Proposed Multilevel with Reduced Number of Switches

known that low dc voltage is generated from photovoltaic systems [1]. Since most of our present electrical systems deal with ac power and for this it is required for dc-ac inverter circuit for efficient power transferring in photovoltaic systems. In order to reduce the harmonic content of the output of the full bridge inverter, various harmonic reduction techniques have to adopt like using passive filters, active filters, SHE PWM, Third Harmonic Elimination etc.

In the scenario, multilevel inverters [12]-[13] can be used which will be able to generate output with reduced harmonic content which can be easily filtered out. In multilevel inverters, numerous power semiconductor switching devices like IGBT, MOSFET etc. is being used which will increase the overall cost and also result in more switching power loss. Basic multilevel inverter topologies like diode-clamped, flying capacitor and cascaded H-bridge [13]-[16] uses more switching devices and other circuit elements. So, with the use of new topologies of multilevel inverter with reduced number of semiconductor switching devices will reduce the cost and overall switching power losses to a great extent. This paper deals with the simulation analysis of a 7-level cascaded H-bridge multilevel inverter and proposed 7-level multilevel inverter topology with reduced number of switches for solar photovoltaic systems.

The Unipolar Single Reference Multicarrier SPWM (U-SR-MC-SPWM) Technique is explained for the proposed inverter. The paper is organized in such a way that section-II gives a general detail about cascaded H-bridge inverter and section-III describes the proposed multilevel inverter topology with reduced number of switches. Simulation results and comparison of Cascaded H-Bridge (using Bipolar-SR-MC-SPWM) and Proposed Inverter (using U-SR-MC-SPWM) are provided in section-IV. Finally, conclusion in provided in section-V.

II. 7-Level Cascaded H-bridge Inverter

Inverters are power electronic converters for efficient conversion of dc-ac power. There are numerous inverter topologies are being developed. For single phase power handling, full bridge inverters are having a more important role. Multilevel inverters [13]-[15] are very important power electronic interface used in photovoltaic systems. Among various multilevel inverters cascaded H-bridge multilevel inverter finds more applications because of its modular structure and absence of capacitors and diode which were present in flying capacitor and diode clamped multilevel inverters. A back to back arrangement of several single phase full bridge inverters results in the formation a cascaded H-

bridge multilevel inverter [13]. In [3], it is mainly discussing about a 7-level cascaded H-bridge multilevel inverter. To form an inverter, which is able generate a 7-level as ac output it is required to connect three single phase full bridge inverters back to back. So, in this total arrangement of the circuit for seven-levels, it requires twelve switching devices like IGBT. If there are '*K*' numbers of sources connected to a cascaded multilevel inverter, then the total number of possible phase voltage level is '*n*' at the output terminals. The relation of *K* and *n* is given by equation (1).

$$n = 2K+1 \quad (1)$$

For a 7-level cascaded multilevel inverter [16], three full bridge inverters will be arranged in back to back. The circuit diagram for seven-level cascaded H-bridge multilevel inverter is shown in Fig. 1. From the circuit, it will be clear that there will be three sources and twelve switching devices for this 7-level topology. By properly giving the gate pulses to the three full bridges it is possible to obtain voltage levels, *+Vdc, +2Vdc, +3Vdc, 0, -Vdc, -2Vdc* and *-3Vdc* for the 7-level cascaded multilevel inverter. In this paper, the gate pulses for the twelve power electronic switches are generated by using Bipolar Single Reference Multicarrier Sinusoidal Pulse Width Modulation (B-SR-MC-SPWM) technique.

III. Seven-Level Proposed Multilevel Inverter with Reduced Number of Switches

Other than the basic multilevel inverter topologies like diode-clamped multilevel inverter, flying-capacitor multilevel inverter [6] and cascaded H-bridge inverter, there are others topologies are also being developed and used in many high-power applications [12]-[16]. As in the earlier section it was discussed that 7-level cascaded H-bridge multilevel inverter requires twelve switching devices for generating seven-level ac output, but by using a proposed multilevel inverter topology it is able to generate seven-level ac output voltage with only nine switching devices. By this reduction of this power semiconductor switching devices, it is able to reduce the cost of the system, reduce the firing circuit requirements and mainly overall switching power losses can be minimized [4]. The circuit topology of multilevel inverter with reduced number of switches is shown in Fig. 2. In this topology, with proper gate pulse generation it is possible to generate seven output voltage levels, *+Vdc, +2Vdc, +3Vdc, 0, -Vdc, -2Vdc* and *-3Vdc*. The switching states in the generation of different voltage levels are given in the Table I.

Table-I 7-Level Multilevel Inverter Switching Pattern.

Output Voltage	Power Semiconductor Switches								
	S1	S2	S3	S4	S5	S6	S7	S8	S9
+Vdc	1	0	0	1	1	0	1	0	1
+2Vdc	1	0	0	1	1	1	0	0	1
+3Vdc	1	0	0	1	1	1	0	1	0
-Vdc	0	1	1	0	1	0	1	0	1
-2Vdc	0	1	1	0	1	1	0	0	1
-3Vdc	0	1	1	0	1	1	0	1	0

Table II Numerical Simulation Parameters for Cascaded and Proposed Multilevel Inverter.

Parameter	Value

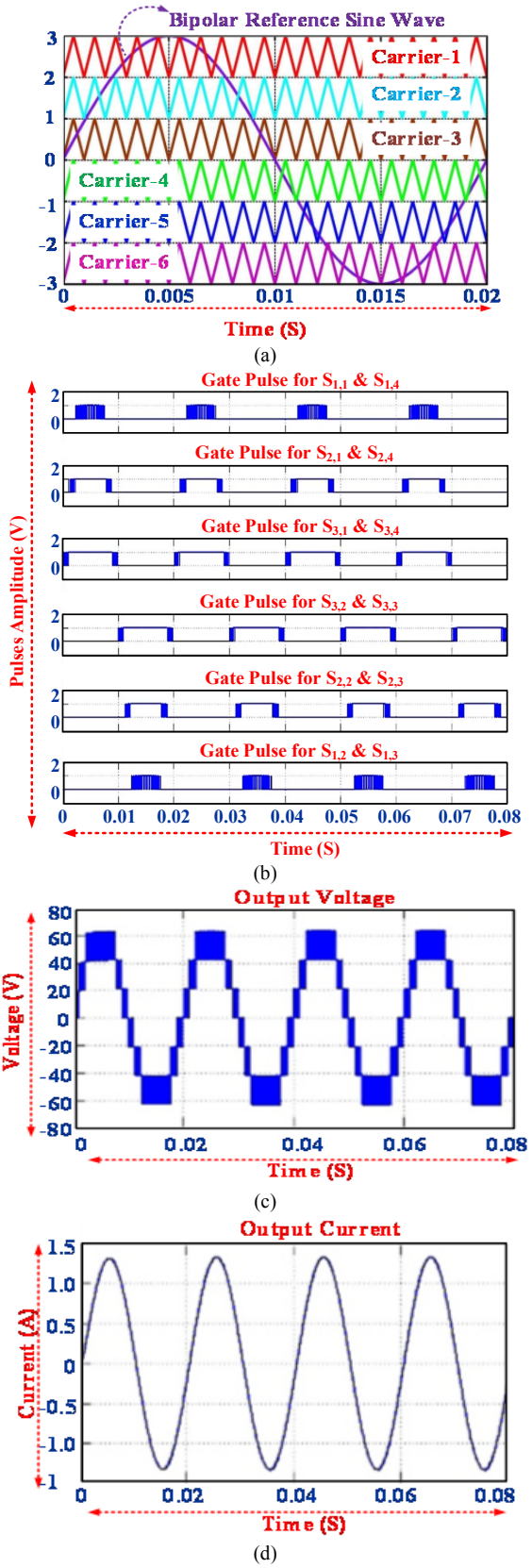
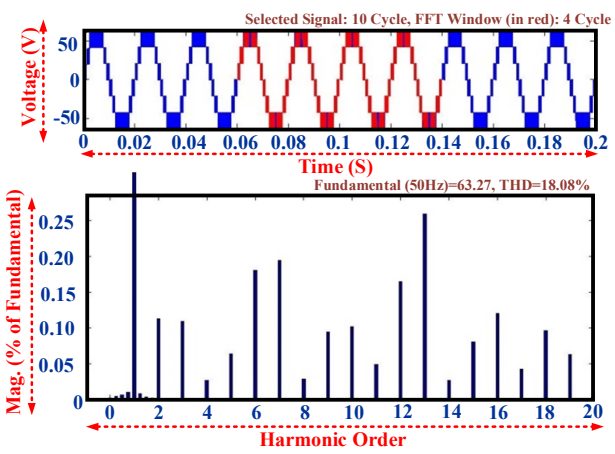
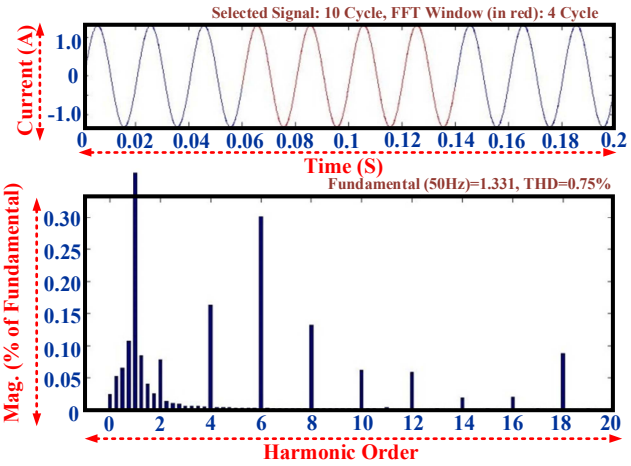


Fig. 3. Simulation Result of cascaded Multilevel Inverter (a) B-SR-MC-SPWM concept (b) Gate pulses (c)7-Level Output Voltage and Output Current



(a)



(b)

Fig. 4. Simulation Results (a) Output voltage harmonic spectrum of cascaded multilevel inverter (b) Output current harmonic spectrum of cascaded multilevel inverter

Output Voltage from each Photovoltaic Panel	21 V
Number of Levels	7
Output Frequency	50 Hz
Power	40W

IV. Simulation Results

Simulation of a seven-level cascaded multilevel inverter and multilevel inverter with reduced number of switches is done in MATLAB/Simulink environment. The parameters used for simulation is given in Table II.

TABLE III Comparison of Cascaded and Proposed Inverter

Inverter Topologies	Voltage THD	Current THD	Number of switches
7-Level Cascaded H-Bridge Inverter	18.08 %	0.75 %	12
7-Level Proposed Inverter	18.35 %	2.18%	09

A. Seven-level Cascaded H-Bridge Multilevel Inverter

7-level cascaded multilevel inverter is simulated in the MATLAB/Simulink environment and the results are discussed in this section. The pulses for the cascaded multilevel inverter are generated using Bipolar Single Reference Multicarrier Sinusoidal Pulse Width Modulation (B-SR-MC-SPWM) technique. The Fig. 3(a) shows the B-SR-MC-SPWM scheme used for the cascaded multilevel inverter and the gate pulses for all the switches which are generated by B-SR-SC-SPWM are shown in Fig. 3(b). The output voltage and current of cascaded multilevel inverter fed from the photovoltaic panel is shown in Fig. 3(c) and Fig. 3(d) respectively. Each photovoltaic panel is supplying a voltage of 21V to the multilevel inverter. The peak value of the output voltage of the multilevel inverter is about 63V and the peak value of the output current is about 1.331A. To analyze the harmonic content in the output voltage and current of cascaded multilevel inverter, FFT analysis is carried out. The harmonic spectrum of output voltage and current is given in the Fig. 4(a) and Fig. 4(b) respectively. The total harmonic distortion of the output voltage of multilevel inverter is about 18.08%. The output current of the cascaded multilevel inverter with the RL load has 0.75% Total Harmonic Distortion.

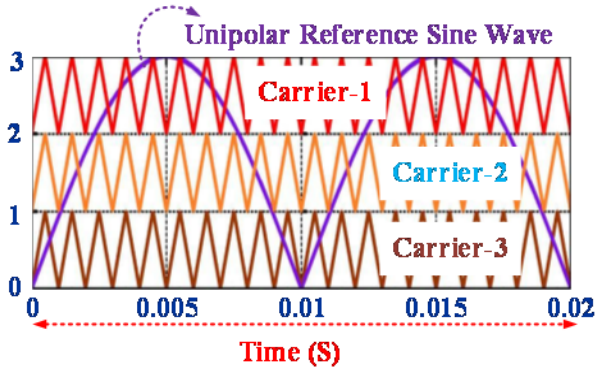


Fig. 5. Concept of U-SR-MC-SPWM for proposed converter

B. Proposed 7-Level Cascaded Multilevel Inverter with Reduced Number of switches.

Proposed 7-level multilevel inverter is simulated is MATLAB/Simulink environment and the results are discussed in this section. The pulses for the multilevel inverter are generated using Unipolar Single Reference Multicarrier Sinusoidal Pulse Width Modulation (U-SR-MC-SPWM) technique. The Fig. 5 shows the U-SR-MC-SPWM concept used for the multilevel inverter with reduced number of switches. The gate pulses for all the switches which are generated by USR-MC-SPWM are shown in Fig. 6(a) and Fig. 6(b). The output voltage and current of the proposed multilevel inverter with reduced number of switches fed from the photovoltaic panel is shown in Fig. 6(c) and Fig. 6(d). Each photovoltaic panel is supplying a voltage of 21V to the multilevel inverter. The peak value of the output voltage of the multilevel inverter is about 63V and the peak value of the output current is about 1.329A. To analyze the harmonic content in the output voltage and current of multilevel inverter, FFT analysis is carried out. The harmonic spectrum of output voltage and current is given in the Fig. 6(e) and Fig. 6(f). The total harmonic distortion of the output voltage of multilevel inverter is about 18.35%. The output current of multilevel inverter with reduced number of switches with RL load has 2.18 % total harmonic distortion. The comparison of

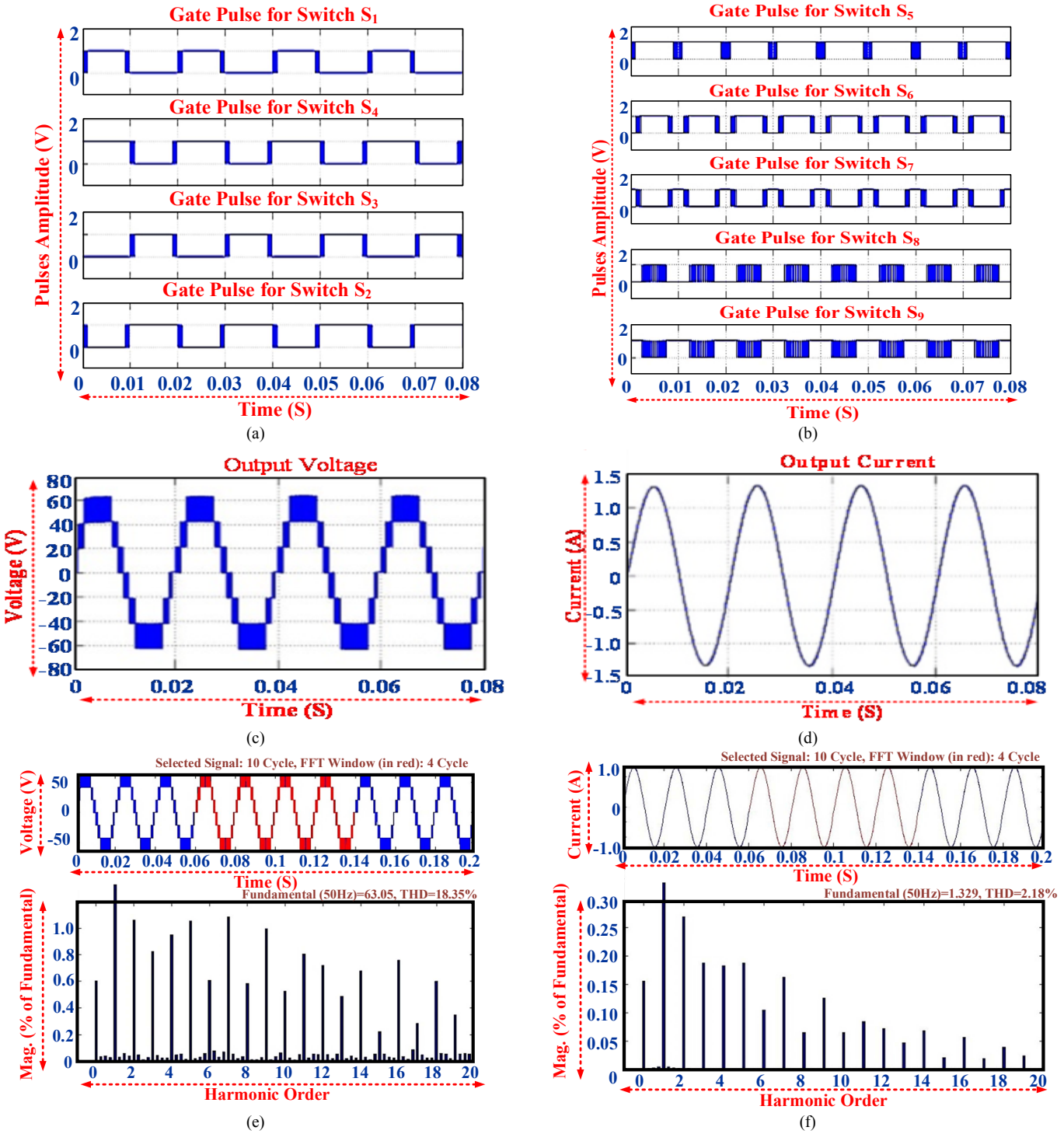


Fig. 6. Simulation result of the proposed multilevel inverter (a) Gate pulses for switches S_1, S_2, S_3 *and* S_4 (b) Gate pulses for switches S_5, S_6, S_7, S_8 and S_9 (c)7-Level Output Voltage (d) Output Current (e) Output voltage harmonic spectrum of proposed multilevel inverter (f) Output current harmonic spectrum of the proposed multilevel inverter.

cascaded and proposed inverter in terms of voltage, current THD is shown in Table III.

V. Conclusion

The paper deals with Unipolar Single Reference Multicarrier Sinusoidal Pulse Width Modulation (U-SR-MC-PWM) for 7-level Inverter with reduced number of power semiconductor switches. The simulation analysis with comparative study of cascaded and proposed multilevel inverters was done in MATLAB/Simulink environment. The harmonic content in both multilevel inverters was analyzed using FFT analysis. The harmonic content in proposed multilevel inverter is slightly greater than that of the

traditional cascaded multilevel inverter. But, in cascaded H-bridge multilevel inverter twelve switching devices are used and in proposed inverter topology only nine switching devices are used for generating seven-level output. This reduction in the semiconductor switching devices, reduces overall system complexity, expenses and switching power losses.

REFERENCES

[1] M. S. Bhaskar, P. Sanjeevikumar, and F. Blaabjerg, "A Multistage DC-DC Step-Up Self-Balanced and Magnetic Component-Free Converter for Photovoltaic Applications: Hardware Implementation", *MDPI Energies*, vol. 10, no. 5, p. 719, May 2017.

[2] M. S. Bhaskar, P. Sanjeevikumar, V. Fedák, F. Blaabjerg, and P. Wheeler, "Transistor Clamped Five-Level Inverter using Non-Inverting Double Reference Sing le Carrier PWM Technique for photovoltaic applications*", Intl. Conf. on Optimization of Electrical and Electronic Equipment (IEEE OPTIM'17) and Intl Aegean Conf. on Electrical Machines and Power Electronics (IEEE ACEMP'17),* Brasov, Romania, pp. 777–782, 25-27 May 2017.

[3] X. Li, D. Zhang, Y. Li, and Y. Xu, "Multi-String Photovoltaic Grid-Connected Inverter Based on Alternate Single-Phase PWM Control", *Conf. Proc. IEEE Asia-Pacific Power and Energy Engineering Conference (IEEE APPEEC'12)*, Shanghai, China, pp. 1–4, 27-29 Mar. 2012.

[4] J. J. Nedumgatt, D. V. Kumar, A. Kirubakaran, and S. Umashankar, "A multilevel inverter with reduced number of switches", *Conf. Proc. IEEE Students' on Electrical, Electronics and Computer Science (IEEE SCEECS'12)*, Bhopal, India, pp. 1–4, 1-2 Mar. 2012.

[5] H. Ghoreishy, A. Y. Varjani, S. Farhangi, and M. Mohamadian, "Hybrid cascaded H-bridge inverter with even power distribution and improved total harmonic distortion: analysis and experimental validation", *IET Power Electron.*, vol. 5, no. 8, pp. 1245–1253, Sep. 2012.

[6] P. Sanjeevikumar, M. S. Bhaskar, P. K. Maroti, F. Blaabjerg, P. Siano, and V. Oleschuk, "Hextuple-inverter configuration for multilevel nine-phase symmetrical open-winding converter", *Conf. Proc. IEEE 1st Intl. Conf. on Power Electronics, Intelligent Control and Energy Systems (IEEE ICPEICES'16),* Delhi, India, pp. 1–6, 4-6 Jul. 2016.

[7] P. Sanjeevikumar, F. Blaabjerg, P. Wheeler, R. Khanna, M. S. Bhaskar, and S. Dwivedi, "Optimized carrier based multilevel generated modified dual three-phase open-winding inverter for medium power application", *Conf. Proc. IEEE Transportation Electrification Conf. and Expo, Asia-Pacific (ITEC Asia-Pacific),* Busan South Korea, pp. 040–045. 1-4 Jun. 2016.

[8] P. Sanjeevikumar, M. S. Bhaskar, F. Blaabjerg, L. E. Norum, S. Seshagiri, and A. Hajizadeh, "Nine-phase hex-tuple inverter for five-level output based on double carrier PWM technique", *4th IET Clean Energy and Tech. Conf., (IET CEAT' 16)*, Kuala Lumpur, Malaysia, pp. 1-7, Jan. 2016.

[9] P. Sanjeevikumar, M. S. Bhaskar, F. Blaabjerg, M. Pecht, L. Martirano, and M. Manganelli, "Dual Six-Phase Multilevel AC Drive with Single Carrier Optimized Five-Level PWM for Star-Winding Configuration", *Lecture Notes on Electrical Engg., Advances in Systems, Control and Automation*, Springer, Singapore, vol. 442, pp. 733–740, Jan 2018.

[10] K. M. Pandav, S. B. Mahajan, P. Sanjeevikumar, S. M. Badave, and R. M. Pachagade, "2.4 kW Three-Phase Inverter for Aircraft Application-Hardware Implementation", *Lecture Notes on Electrical Engg., Advances in Power Systems and Energy Management*, Springer, Singapore, vol. 436, pp. 325–335, Jan 2018.

[11] M. G. Villalva, J. R. Gazoli, and E. R. Filho, "Comprehensive Approach to Modeling and Simulation of Photovoltaic Arrays", *IEEE Trans. on Power Electron.*, vol. 24, no. 5, pp. 1198–1208, May 2009.

[12] P. Sanjeevikumar, P. Siano, A. H. Ertas, R. Selvamuthukumaran, and P. K. Maroti, "Single-phase seven-level stack multicell converter using level shifting SPWM technique", *Conf. Proc. IEEE 16th Intl. Conf. on Environment and Electrical Engg., (IEEE EEEIC'16),* Florence, Italy, pp. 1–5, 7-10 June 2016.

[13] S. Rivera, S. Kouro, B. Wu, J. I. Leon, J. Rodríguez, and L. G. Franquelo, "Cascaded H-bridge multilevel converter multistring topology for large scale photovoltaic systems", *Conf. Proc. IEEE Intl. Symposium on Ind. Electron., IEEE ISIE'11*, Gdansk, Poland, pp. 1837–1844, 27-30 June 2011.

[14] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. Franquelo, B. Wu, J. Rodriguez, M. Perez, J. Leon "Recent Advances and Industrial Applications of Multilevel Converters", *IEEE Trans. on Ind. Electron.,* vol. 57, no. 8, pp. 2553–2580, Aug. 2010.

[15] N. A. Rahim and J. Selvaraj, "Multistring Five-Level Inverter with Novel PWM Control Scheme for PV Application", *IEEE Trans. on Ind. Electron.*, vol. 57, no. 6, pp. 2111–2123, Jun. 2010.

[16] E. Villanueva, P. Correa, J. Rodriguez, and M. Pacas, "Control of a Single-Phase Cascaded H-Bridge Multilevel Inverter for Grid-Connected Photovoltaic Systems", *IEEE Trans. on Ind. Electron.*, vol. 56, no. 11, pp. 4399–4406, Nov. 2009.