Influence of Emitter Side Design on the Unintentional Turn-on of 10kV+ SiC n-IGBTs

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***Abstract*— Silicon Carbide (SiC) N-channel Insulated Gate Bipolar Transistors (n-IGBTs) rated higher than 10kV can improve Medium Voltage and High Voltage power electronics due to the favourable combination of SiC material with the n-IGBT device structure. This paper investigates the phenomenon of unintentional turn-on occurring due to high dV/dt produced during switching transients and analyses the impact of design parameters such as the channel length, the p-well doping and the oxide thickness for their ability to suppress it.**

Keywords— SiC IGBT, unintentional turn-on, coupling noise

I. INTRODUCTION

Ultra-high voltage switching devices rated 10kV+ have attracted significant interest because of an increased demand to condition with power electronics vast amounts of electrical power, e.g. from renewable energy generation sites. SiC n-IGBTs seem to be the most appropriate for use in such voltage ranges (above 10kV) because of the superior performance characteristics of SiC and the conductivity modulation achieved in IGBT structures [1]. Therefore, SiC IGBT-based converters can offer significant benefits in terms of efficiency, complexity, and cooling requirements for HVDC applications compared to the multilevel silicon counterparts [2].

Recent studies have shown that the performance of the ultra-high voltage n-IGBT can be improved by using a retrograde doping profile in the p-well [3]. This approach was initially proposed for the low-power CMOS technology to improve various electrical characteristics such as punch-through of the emitter region during blocking state, latch-up and threshold voltage [4], but lately also used in high voltage SiC devices. Additionally, the lower energy implantation required for the retrograde p-well compared with the conventional approach can reduce the lattice damage at the surface of the semiconductor, leading to reduced leakage current and increased carrier mobility [5], [6].

Extensive simulations presented in [3], [7], [8] concluded that the optimally designed retrograde p-well can eliminate the punch-through of the emitter region and achieve robust control on the threshold voltage by increasing the oxide thickness. The latter is of great importance and enhances the long-term reliability of MOS devices. However, the high dv/dt of the PT-IGBT during switching transients [9] and the reduced gate capacitance due to the increased oxide thickness leads to a higher possibility of unintentional turn-on and eventually loss of control over the gate electrode or increased switching losses. This phenomenon has been studied in lower voltage devices in e.g. leg-configuration topologies where the devices are intended to turn on with appropriate dead times [10].

In response to this, various solutions have been proposed, including the usage of negative gate bias, different gate resistors for the turn-on and turn-off transients or external gate capacitors [11]. Additionally, advanced gate drivers offer active Miller clamping or digitally controlled active gate driving to reduce the switching slope and to protect the device in a failure event before it is permanently destroyed [12]. However, these correction techniques add complexity and put limitations, especially in power modules where passive and semiconductor components need to be integrated into the same package [13].

This paper analyses the inductive turn-off process of 10kV rated IGBTs using isothermal TCAD simulations, discusses the origin of high dV/dt and the spike in the gate voltage, assesses the impact of various design variables on the unintentional turn-on robustness and aims to mitigate it at the device level.

The rest of this paper is organised as follows. Section II presents the TCAD modelling approach and the simulation test setup. The inductive turn-off process of the IGBT is analysed in Section III, and the mechanism of gate voltage spike generation is presented in Section IV. Different device parameters are varied in Section V, and their effects on the unintentional turn-on robustness are discussed. Finally, Section VI concludes the paper.

II. DEVICE STRUCTURE, MODELING AND SIMULATION

A SiC n-IGBT half-cell is shown in Fig. 1(a). The doping concentration of the p+ injector, n buffer layer and n- drift layer are 1×10^{19}, 5×10^{17} and 3×10^{14} $cm^{-3,}$ respectively. The thicknesses are 4, 3 and 100 μm, respectively. The doping profile of the p-well is retrograde, featuring a lower surface doping which can be adjusted, a maximum doping

concentration of 2×10^{18} cm^{-3} at a depth of 0.5 μm which then gradually reduces to 3×10^{14} cm^{-3} at a depth of 2 μm. This profile addresses possible punch-through of the emitter region, prevents parasitic thyristor latch-up and decouples the oxide thickness from the gate threshold voltage and the blocking capability. Therefore, the oxide thickness can be increased, e.g. offering higher long-term device reliability. The above values achieve a breakdown voltage of about 13.5kV at room temperature (Fig. 1(b)), thus allowing to class the device at 10kV.

The oxide thicknesses (t_{ox} and t_{IE}), channel and JFET length and surface doping of the retrograde p-well were varied by altering the process conditions, allowing to study their impact on the device characteristics. Sentaurus TCAD was used to simulate the fabrication procedure (process simulation) and the dynamic performance of the device in a chopper topology (mixed-mode simulation of a finite element device surrounded with a SPICE representation of the circuit) shown in Fig. 1(c). The simulations use previously calibrated models for critical semiconductor physics, including incomplete ionisation, impact ionisation, Shockley-Read-Hall (SRH) and Auger recombination, doping and temperature dependence and anisotropy of mobility, fixed charge and interface traps at the oxide – semiconductor interface [3], [14].

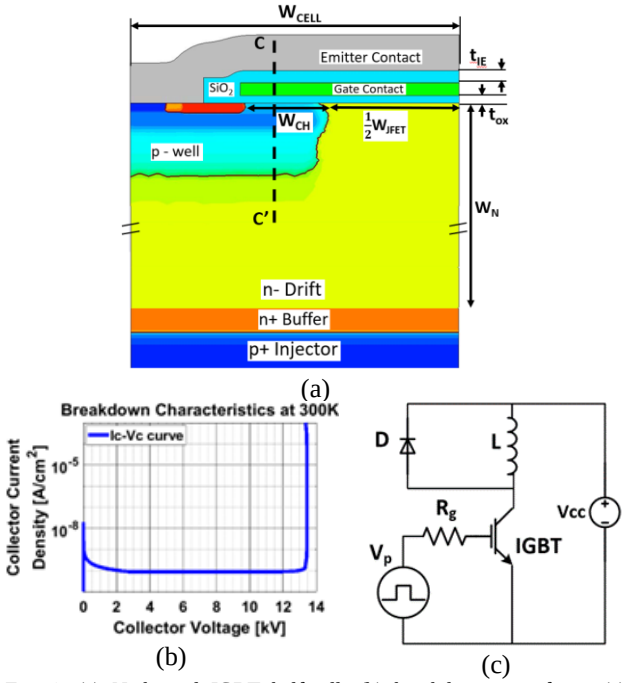

Fig. 1. (a) N-channel IGBT half-cell; (b) breakdown waveform; (c) chopper circuit topology.

III. Voltage Rise Explanation During the Turn-off Process of Silicon Carbide IGBT

The SiC IGBTs exhibit two different voltage rising phases, a slow and a fast, as has been already demonstrated in various papers [15]–[21]. An explanation of them will help understand the origins of the high dV/dt.

At the beginning of the turn-off process, the space charge region starts expanding towards the collector side by removing holes at the space charge boundary. According to the charge control principle, the charge removed by the expansion of the space charge region must be equal to the charge removed due to the collector current flow [22] given by Eq. 1.

$$J_{C,ON} = q \cdot p_{SC,boundary}(t) \frac{dW_{SC}(t)}{dt} \quad (1)$$

By integrating this equation and applying the boundary conditions as explained in [22], the evolution of the space charge region width with time can be given by Eq. 2:

$$W_{SC}(t) = L_a acosh\left\{\frac{J_{C,ON}\sinh\left[\frac{W_N+W_{NB}}{L_a}\right]}{qL_a p(W_{NB+})}\, t + \cosh\left[\frac{W_{SC}(0)}{L_a}\right]\right\} \quad (2)$$

Where L_a is the ambipolar diffusion length in the drift region, $W_{SC}(0)$ the space charge region width at the beginning of the turn-off process and $p(W_{NB+})$ is the hole density in the boundary between the drift and buffer layer.

The collector voltage is related to the space charge width by Eq. 3, where the positive charge in the space charge region due to the collector current flow has been taken into account. This positive charge is given by Eq. 4, assuming that the holes are moving at their saturation drift velocity due to the high electric field in the space charge region.

$$V_c(t) = \frac{q(N_d + p_{SC})W_{SC}^2(t)}{2\varepsilon_s} \quad (3)$$

$$p_{SC} = \frac{J_{C,ON}}{q v_{sat,p}} \quad (4)$$

As a result, the space charge width and collector voltage are increasing at a slow pace determined by the injected hole concentration ($p(W_{NB+})$) and the total current density. Additionally, the slope of the electric field is constant according to Poisson's equation 5:

$$\frac{dE}{dx} = \frac{\rho}{\varepsilon_s} = \frac{q(N_d + p_{SC})}{2\varepsilon_s} \quad (5)$$

The slow voltage rising phase ends when the space charge region reaches the buffer layer. The voltage at which the space charge region reaches the buffer layer (Punch-Through voltage V_{PT}) is given by Eq. 3, where replacing the Wsc(t) with W_N. After that time, the electric field slope increases according to Eq. 5 due to the higher doping density of the buffer layer and the Electric field takes a trapezoidal shape.

The time required for the collector voltage to reach the DC bus voltage can be given by integrating the charge control principle equation (Eq. 1), applying boundary conditions at the beginning and end of the second phase of the voltage-rising period, leading to Eq. 7:

$$\Delta t = \frac{q}{J_{C,ON}} \Delta W_{SC,buffer}[p(starting) - p(ending)] \quad (6)$$

Where, $p(starting) - p(ending)$ is the charge to be removed during this period and $\Delta W_{SC,buffer}$ is the depletion region width inside the buffer layer calculated by Eq. 3 using $N_d = N_{BL}$ and $\Delta V_c = (V_{cc} - V_{PT})$.

The origin of the high dV/dt can be explained by examining the hole density at the beginning and ending of the high voltage rising phase in Fig. 2(b). In this figure, the hole density and electric field at the beginning and ending of the fast voltage rising phase are shown with red and green, respectively. As expected by the analytical description above, the space charge region width and the amount of holes to be removed are small, leading to a fast voltage transient.

Figure 2(a) shows the collector and gate voltages and the total, electron and hole current density during the inductive turn-off. The electron current density falls to zero when the gate voltage falls below the threshold voltage. However, as the total current remains constant until the collector voltage reaches the DC bias voltage, the hole current component increases.

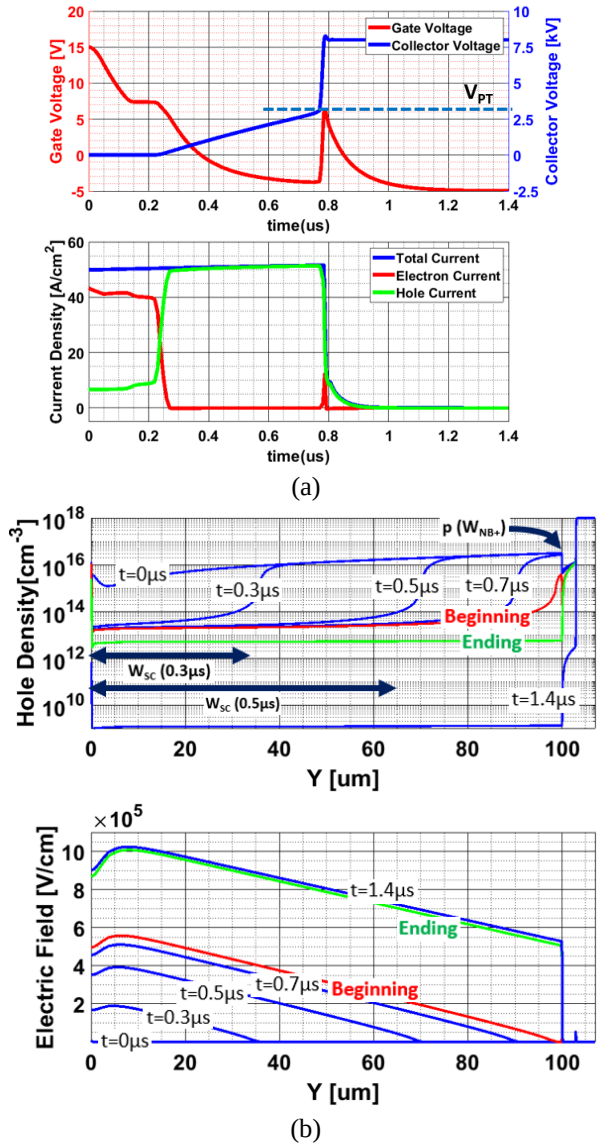

Fig. 2. (a) Gate and collector voltage (top), total, electron and hole current density during inductive turn-off; (b) The hole distribution and Electric field at various instants during the turn-off procedure. The red lines represent the time at the beginning of the high dV/dt phase and the green at the end.

IV. Coupling Noise And Unintentional Turn-On Explanation

The coupling noise between the high-side (HS) and low-side (LS) switching components in a bridge-leg configuration (Fig. 3 a, b) can give a positive and a negative voltage spike in the gate of the LS MOSFET/IGBT during the turn-off and turn-on transient of the HS MOSFET/IGBT. Although both voltage spikes stress the oxide and cause reliability issues, the positive spike can cause unintentional turn-on, leading to increased switching losses, short-circuiting the V_{cc} or even the destruction of the device.

Figure 3(c) shows the simplified equivalent IGBT Resistor-Capacitor (RC) circuit (during switching). The differential equation which describes the relationship between the gate and collector voltage is Eq. 7, and assuming that the dV_c/dt value during the fast voltage rising phase is constant and is given by Eq. 8, a simplified solution of the gate voltage spike is given by Eq. 9. The Δt in these equations is the duration of the fast voltage rising period given by Eq. 6. It can be concluded that a higher gate – emitter capacitance (C_{ge}), and a lower gate resistance (R_g) can improve the unintentional turn-on robustness because they reduce the amplitude of the gate voltage spike. This conclusion could also be drawn directly from the circuit diagram in Fig. 3(c) due to the fact that the impedance of the R_g-C_{ge} parallel connection reduces.

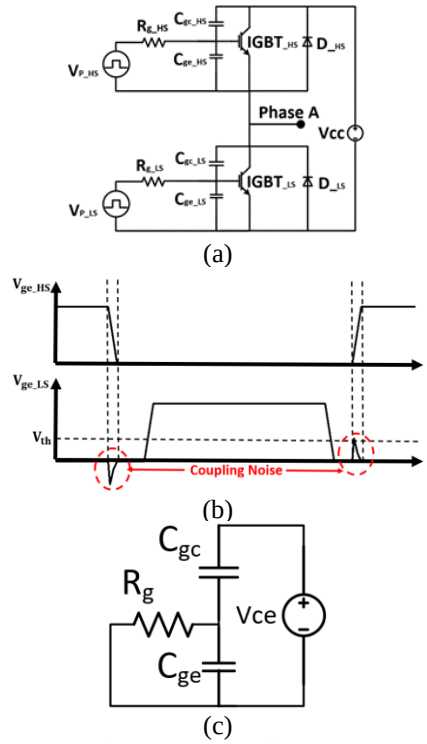

Fig. 3. (a) Simplified bridge-leg configuration; (b) timing diagram showing the coupling noise induced in the gate of the low-side IGBT during the switching transients of the high-side IGBT; (c) equivalent IGBT RC circuit (during switching).

$$\frac{dV_{ge}}{dt} + \frac{1}{(C_{gc,sp}+C_{ge,sp})\cdot R_g} V_{ge} = \frac{C_{gc,sp}}{(C_{gc,sp}+C_{ge,sp})} \cdot \frac{dV_{ce}}{dt} \quad (7)$$

$$\frac{dV_{ce}}{dt} = \frac{\Delta Vc}{\Delta t} = \frac{V_{cc} - V_{PT}}{\Delta t} \quad (8)$$

$$V_{spike} = C_{gc,sp} R_g \frac{V_{cc} - V_{PT}}{\Delta t}\left[1 - e^{-\frac{\Delta t}{(C_{gc,sp}+C_{ge,sp})R_g}}\right] \quad (9)$$

When the gate voltage spike is high, the gate voltage might increase above the threshold voltage. Therefore, there is electron current injection through the channel, as seen in Fig. 4(a). However, because the total current is constant, the hole current component reduces, and thus the hole carrier removal becomes slower. Consequently, the collector voltage changes slope again due to the unintentional turn-on of the channel. Figure 4(b) shows the internal current distribution (total, electron and hole) at the beginning of the turn-off process (t1), at the slow voltage rising period when the channel is turned-off (t2), and during the un-intentional turn-on (t3). The

electron current distribution at t3 shows the electron current injection from the channel.

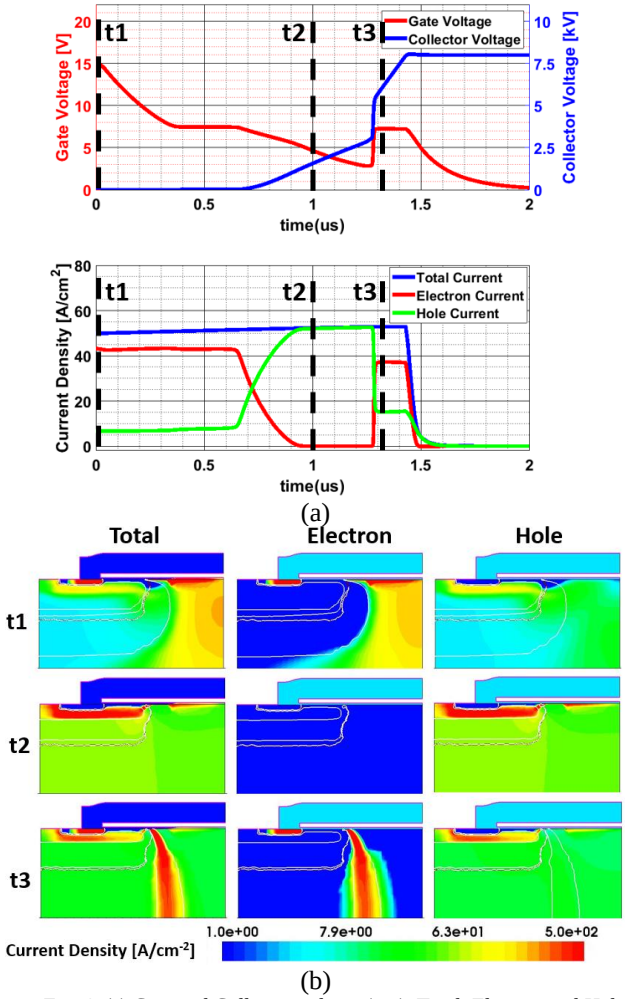

Fig. 4. (a) Gate and Collector voltage (top). Total, Electron and Hole current density (bottom-) ; (b) Total electron and hole current distribution within the device at the beginning of the turn-off process (t1), during the slow voltage rising period (t2) and during the unintentional turn-on (t3).

V. Results And Discussion

The above analysis explained the origins of the high dV/dt and gate voltage spike generation. This section will present how the retrograde p-well profile can be used for independent control of the threshold voltage and gate capacitance, and therefore preventing unintentional turn-ONs. Additionally, it will show the impact of the gate resistance, device temperature and collector current density on the gate voltage spike amplitude.

A. Threshold Voltage and Gate Capacitance Adjustment

The retrograde p-well design allows for a specific threshold voltage to be achieved at different values of gate electrode oxide thickness t_{ox} when concurrently adjusting the p-well surface doping, from 5×10^{16} cm^{-3} to 5×10^{17} cm^{-3}. As shown in Fig. 5, when keeping the surface doping concentration fixed at about 5×10^{16} cm^{-3} and increasing the t_{ox} (Fig. 5(a)), the threshold voltage also increases. However, the combination of p-well surface doping values shown in Fig. 5(c - d) and t_{ox} values in Fig. 5(b) give approximately the same threshold voltage of 5.5V, chosen to be neither too small to increase the noise immunity of the device nor too high for long-term gate oxide reliability. As a result, this special doping profile of the p-well allows the independent adjustment of the threshold voltage and the gate capacitance.

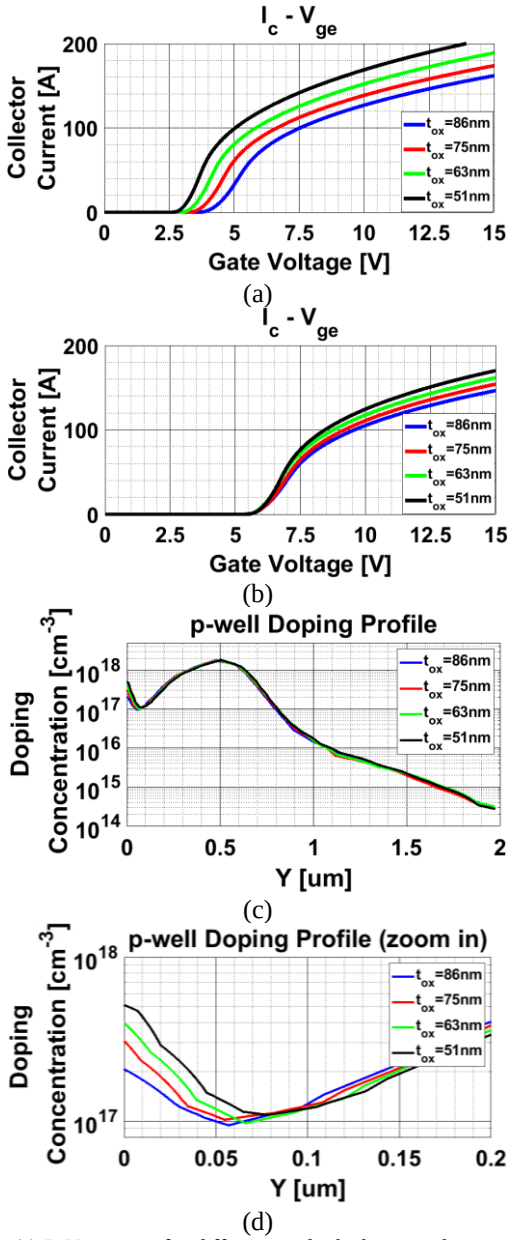

Fig. 5. (a) I_c-V_{ge} curves for different oxide thickness and same surface doping concentration; (b) I_c-V_{ge} curves for different oxide thickness and different surface doping concentrations; (c) doping concentration profile for the cases shown in (b); (c) doping concentration profile for the cases shown in (b) at the surface.

The above-mentioned combinations of oxide thickness and doping profile were carried forward for further assessments, where the channel length (W_{ch}), JFET length (W_{JFET}) and intermetal oxide (t_{IE}) were also varied. To keep the half-cell pitch constant at 9µm, the sum of the W_{ch} and (½)W_{JFET} was kept constant at 6µm. Thus (½)W_{JFET}= 6 - W_{ch}. The dynamic response of the IGBT was assessed at 50 Acm^{-2} (inductive) and testing voltage 8kV with a gate driving voltage of 15V for all cases. Additionally, negative gate bias (-5V) is used for the turn-off to increase the noise immunity of the IGBT without adding significant complexity to the gate driving circuit.

According to Eq. 9, the gate-to-emitter capacitance has a direct influence on the gate voltage spike and, as a result, can

be optimised in order to reduce it. The Gate-to-Emitter capacitance is determined by the overlap between the gate contact and the P-well and n++ region, and the intermetal capacitance between the gate and emitter electrodes, as shown in Fig. 6.

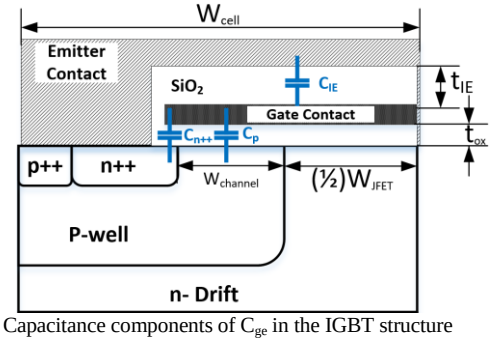

Fig. 6. Capacitance components of C_{ge} in the IGBT structure

Equation 10 gives the total gate-to-emitter capacitance and can be related to the device's geometry according to Eq. 11. In this equation, the C_{n++} component is very small and can be neglected.

$$C_{ge,sp} = C_p + C_{n++} + C_{IE} \tag{10}$$

$$C_{ge,sp} = \frac{W_{channel}}{W_{cell}} \cdot \frac{\varepsilon_{SiO_2}}{t_{ox}} + \frac{W_{channel} + W_{JFET}}{W_{cell}} \cdot \frac{\varepsilon_{SiO_2}}{t_{IE}} \tag{11}$$

Fig. 7(a)-(c) shows the influence of variations in channel length ($W_{channel}$), gate oxide (t_{ox}) and intermetal oxide (t_{IE}) on the gate voltage spike. The results are in agreement with the analysis presented above.

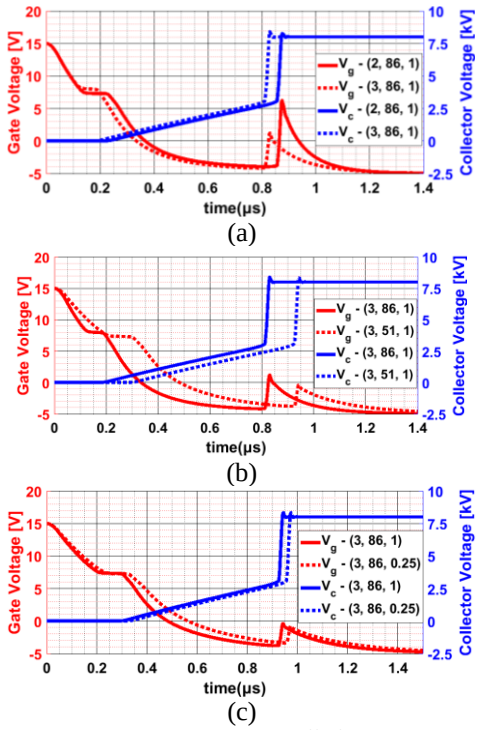

Fig. 7. $V_c(t)$ and $V_g(t)$ during the turn-off of SiC n-IGBTs having (a) different W_{ch}, (b) different t_{ox}, and (c) different t_{IE}; The values inside the legend parenthesis denote for (W_{ch} [µm], t_{ox}[nm], t_{IE}[µm]).

Table I summarises the impact of the gate capacitance variation on the on-state voltage drop, turn-off switching losses, gate voltage spike and dV/dt values for the above cases. It can be seen that the gate voltage spike was reduced by 78% by only increasing the on-state voltage drop by 15%. However, this gate voltage spike suppression allows for significant gate threshold voltage reduction, and thus lower on-state voltage drop can be achieved for the same gate voltage.

TABLE I. ELECTRICAL CHARACTERISTICS OF IGBTS WITH DIFFERENT EMITTER SIDE DESIGNS

$W_{channel}$ [µm]	t_{ox} [nm]	t_{IE} [µm]	V_{on} [V]	E_{off} [mJ]	dV/dt [kV/µs]	V_{spike} [V]
2	86	1	3.95	53	396	10.26
3	86	1	4.88	52	431	5.3
3	51	1	4.74	52	422	3.37
3	51	0.25	4.64	53	414	2.26

B. Gate resistance variation

Figure 8 shows the transient waveforms for an IGBT with (W_{ch} [µm],t_{ox}[nm], t_{IE} [µm]) = (2,86,1) when using 2.5Ω, 7.5Ω and 30Ω gate resistor. It can be seen that the voltage spike increases with the increase of the gate resistance. Especially for the 30Ω case, the gate voltage (Fig. 8(a)) rose above the threshold voltage leading to unintentional turn-on indicated by the channel current rise (I_{ch} in Fig. 8(b)) at the fast-rising phase of the collector voltage. This had the result of increased turn-off switching duration and losses. If this occurs in a bridge-leg configuration (Fig. 3(a)), it will result in a short-circuit of the V_{cc} and operation of the IGBT in short-circuit conditions.

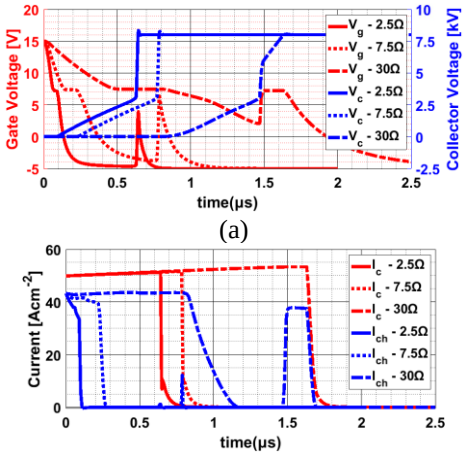

Fig. 8. (a) $V_c(t)$ and $V_g(t)$; (b) $I_c(t)$ and $I_{ch}(t)$ for different gate resistances.

C. Impact of Collector Current Density

Figure 9 shows the gate and collector voltage during the IGBT turn-off at different collector current densities. As can be seen, the gate voltage spike reduces as the current density increases because the PT voltage increases and thus the ΔV in Eq. 8,9 reduces.

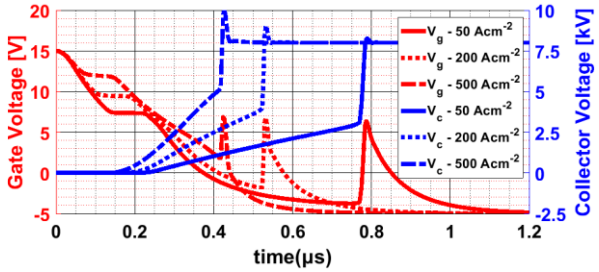

Fig. 9. $V_c(t)$ and $V_g(t)$ during the IGBT turn-off at different collector current densities

D. *Impact of Temperature*

Finally, the temperature dependence of the gate voltage spike is shown in Fig. 10, where the IGBT is turned-off at temperatures between 373K and 500K. It can be seen that the gate voltage spike is relatively unaffected by the temperature variation. The slight voltage spike reduction at higher temperatures can be explained by the fact that the plasma injection is enhanced, and thus more holes need to be removed from the buffer layer during the fast voltage rising period, which means that the dV/dt reduces.

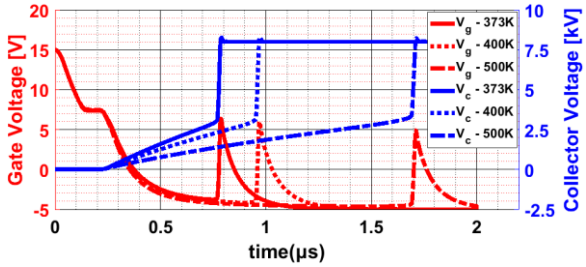

Fig. 10. $V_c(t)$ and $V_g(t)$ during the IGBT turn-off at different collector current densities

VI. CONCLUSIONS

The influence of emitter side design on the unintentional turn-on of SiC n-IGBTs rated 10kV+ was investigated with process and mixed – mode (device – circuit) TCAD simulations. The phenomenon can increase the losses but can also lead to operation under short circuit conditions which can be catastrophic; it should hence be suppressed. It was shown that the gate voltage spike responsible for the unintentional turn-on reduces by adjusting the gate oxide thickness and channel length; due to the influence of these design parameters on the gate – emitter capacitance. Further, the doping profile of a retrograde p-well can be tweaked to maintain the gate threshold voltage, oxide reliability and overall performance to the desired level. Consequently, the immunity of 10kV+ rated SiC n-IGBTs to turn on unintentionally during switching can be adjusted via an appropriate design of the emitter side.

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